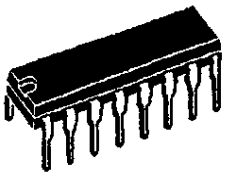
EXHIBIT 1

SGS-THOMSON MICROELECTRONICS

TEA2262

SWITCH MODE POWER SUPPLY CONTROLLER

- POSITIVE AND NEGATIVE OUTPUT CURRENT UP TO 1A
- LOW START-UP CURRENT
- DIRECT DRIVE OF THE MOS POWER TRANSISTOR
- TWO LEVELS TRANSISTOR CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- SOFT-STARTING
- UNDER AND OVERVOLTAGE LOCK-OUT
- AUTOMATIC STAND-BY MODE
- LARGE POWER RANGE CAPABILITY IN STAND-BY (Burst mode)
- INTERNAL PWM SIGNAL GENERATOR



DIP16
(Plastic Package)

ORDER CODE : TEA2262

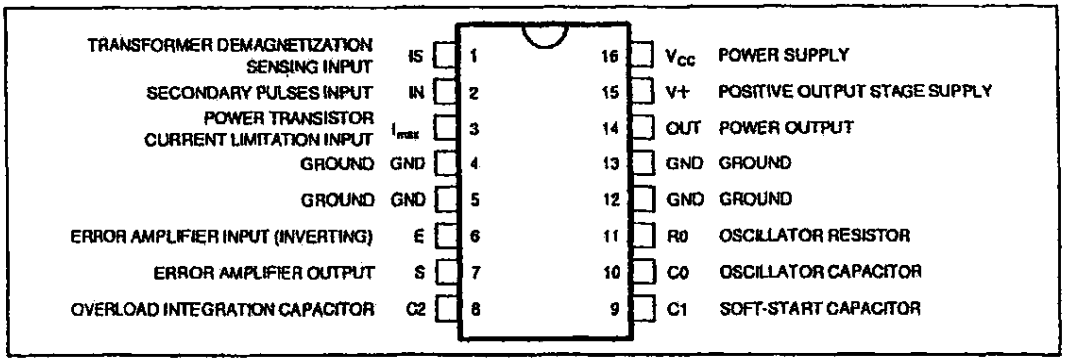
DESCRIPTION

The TEA2262 is a monolithic integrated circuit for the use in primary part of an off-line switching mode power supply using a MOS power transistor.

All functions required for SMPS control under normal operating, transient or abnormal conditions are provided.

The capability of working according to the "master-slave" concept, or according to the "primary regulation" mode makes the TEA2262 very flexible and easy to use. This is particularly true for TV receivers where the IC provides an attractive and low cost solution (no need of stand-by auxiliary power supply).

PIN CONNECTIONS



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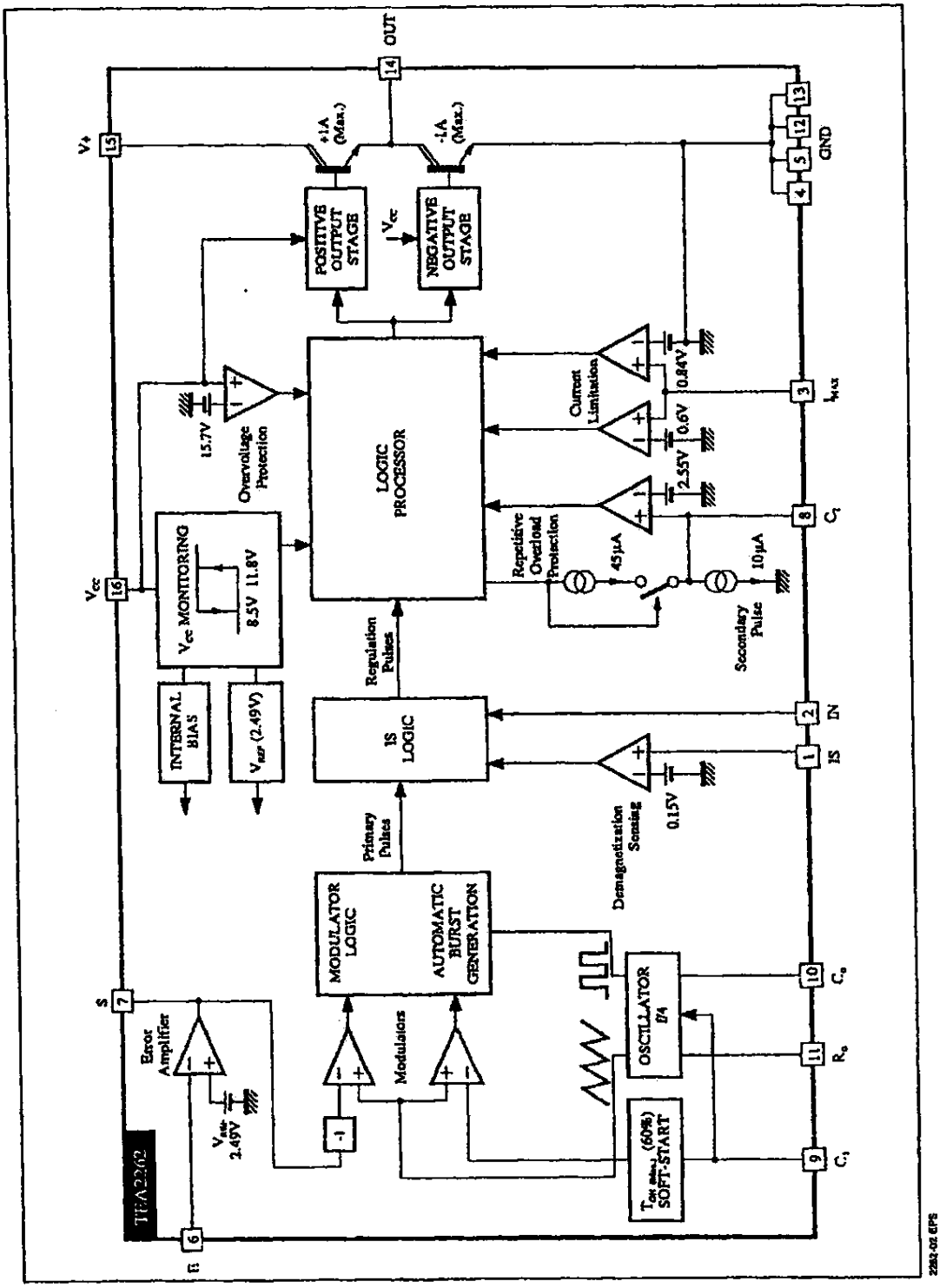
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Power Supply	V16-V4, 5, 12, 13	20	V
V+	Output Stage Power Supply	V15-V4, 5, 12, 13	20	V
I_{OUT+}	Positive Output Current (source current)		1.5	A
I_{OUT-}	Negative Output Current (sink current)		1.5	A
T_j	Operating Junction Temperature		150	°C
T_{stg}	Storage Temperature		-40, +150	°C

2262-01 TBL

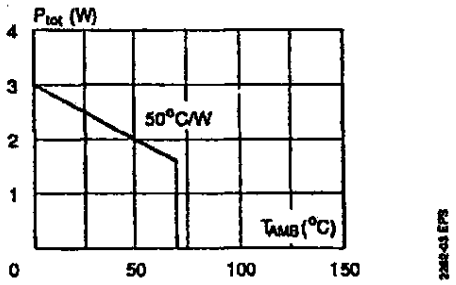
THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	15	°C/W
$R_{th\ (j-a)}$*	Junction-ambient Thermal Resistance	50	°C/W

2262-02 TBL

* Soldered on a 35µm, 40cm² board copper area

Figure 1 : Maximum Power Dissipation



2262-03 EPS

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	V_{CC} stop	12	V_{CC} max	V
I_{OUT+}	Positive Output Current (source current)			1	A
I_{OUT-}	Negative Output Current (sink current)			1	A
I_{OUT+}	Average Positive Output Current			0.3	A
I_{OUT-}	Average Negative Output Current			0.3	A
f_{oper}	Operating Frequency	10		150	kHz
V_{IN}	Input Pulses Amplitude (Pin 2)	1.5	2.5	4.5	V
R_{OSC}	Oscillator Resistor Range	10		100	kΩ
C_{OSC}	Oscillator Capacitor Range	0.33		4.7	nF
C1	Soft-starting Capacitor Range	0.047	1		µF
C2	Overload Integration Capacitor	0.047	1		µF
C2/C1	Ratio C2/C1 (C2 must be ≥ C1)	1			
T_{amb}	Operating Ambient Temperature	-20		70	°C

2262-03 TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} =12V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLY					
$V_{CC(start)}$	Starting Voltage (V_{CC} increasing)	9.5	11.8	13	V
$V_{CC(stop)}$	Stopping Voltage (V_{CC} decreasing)	7	8.5	9.5	V
Hyst V_{CC}	Hysteresis ($V_{CC(start)}$ - $V_{CC(Stop)}$)	2.7	3.3	3.7	V
$I_{CC(start)}$	Starting Current (V_{CC} = 9V)		0.5		mA
I_{CC}	Supply Current (V_{CC} = 12V)		6.5		mA
$V_{CC(max)}$	Overvoltage Threshold on V_{CC}	15	15.7		V
$I_{CC(over)}$	Supply Current after Overvoltage Detection (V_{CC} = 17V)		35		mA
OSCILLATOR / PWM SECTION					
$\frac{\Delta F}{F}$	Accuracy (R_{OSC} = 68kΩ, C_{OSC} = 1nF)		10		%
t_{ON} max	Maximum Duty Cycle in Primary Regulation Mode	50	60	70	%
ERROR AMPLIFIER SECTION					
A_{VO}	Open Loop Gain		75		dB
F_{ug}	Unity Gain Frequency		550		kHz
I_{SC}	Short Circuit Output Current (Pin 7 connected to ground)		2		mA
I_{BE}	E Input Bias Current (Pin 6)		0.08		µA
V_{REF}	Internal Voltage Reference (connected to error amplifier input and not directly accessible)	2.34	2.49	2.64	V
INPUT SECTION					
V_{IN}	IN Input Threshold (Pin 2)	0.6	0.85	1.2	V
V_{IS}	IS Input Threshold (Pin 1)		0.15		V
I_{BIN}	IN Input Bias Current		0.3		µA
I_{BIS}	IS Input Bias Current		0.4		µA
CURRENT LIMITATION SECTION					
V_{IM1}	First Current Limitation Threshold	550	600	650	mV
V_{IM2}	Second Current Limitation Threshold	780	840	900	mV
ΔV_{IM}	Thresholds Difference V_{IM2} - V_{IM1}	190	240	280	mV
V_{C2}	Lock-out Threshold on Pin C2	2.25	2.55	2.85	V
I_{DC2}	Capacitor C2 Discharge Current		10		µA
I_{CC2}	Capacitor C2 Charge Current		45		µA
$I_{BI(max)}$	Maximum Input Bias Current (Pin 3)		0.2		µA

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SIMPLIFIED APPLICATION DIAGRAMS

Figure 1 : Master-slave Concept

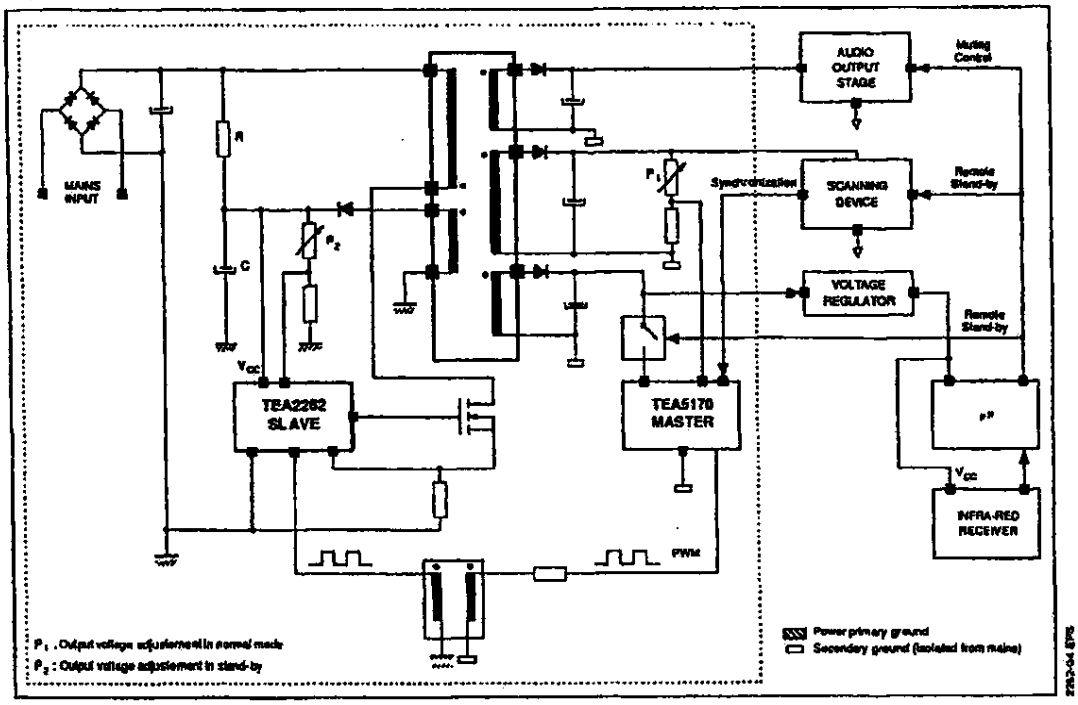
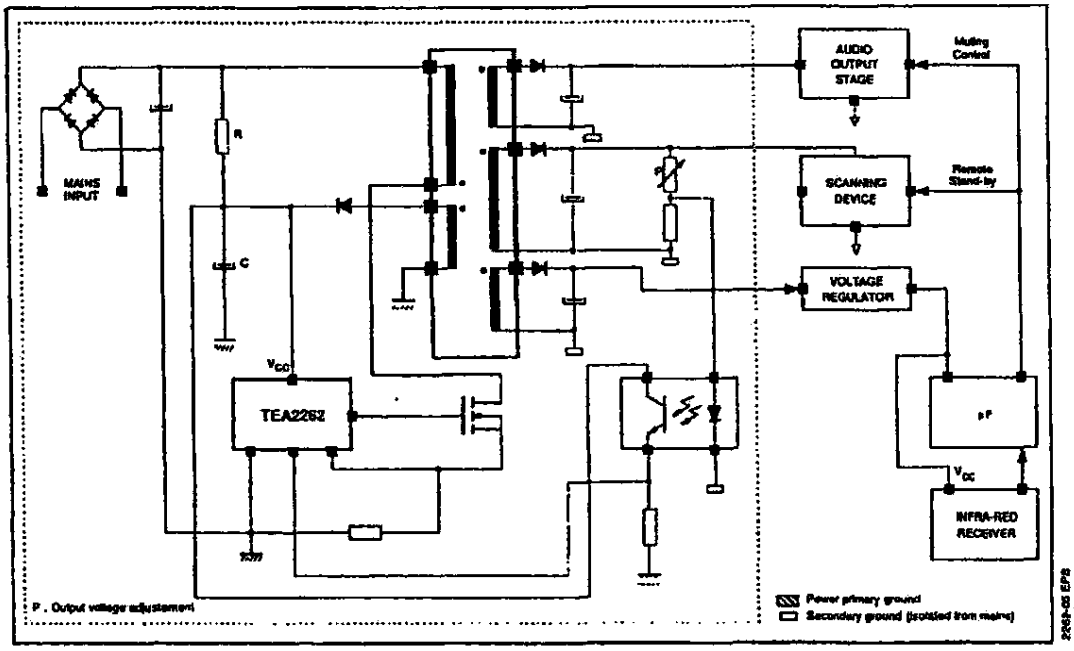


Figure 2 : Secondary Regulation (with optocoupler)



GENERAL DESCRIPTION

The TEA2262 is an off-line switch mode power supply controller. The synchronization function and the specific operation in stand-by mode make it well adapted to video applications such as TV sets, VCRs, monitors, etc...

The TEA2262 can be used in two types of architectures :

- Master/slave architecture. In this case, the TEA2262 drives the power transistor according to the pulse width modulated signals generated by the secondary located master circuit. A pulse transformer provides the feedback (see Figure 1).
- Conventional architecture with linear feedback signal (feedback sources : optocoupler or transformer winding) (see Figure 2).

Using the TEA2262, the stand-by auxiliary power supply, often realized with a small but costly 50Hz transformer, is no longer necessary. The burst mode operation of the TEA2262 makes possible the control of very low output power (down to less than 1W) with the main power transformer.

When used in a master/slave architecture, the TEA2262 and also the power transistor turn-off can be easily synchronized with the line transformer. The switching noise cannot disturb the picture in this case.

As an S.M.P.S. controller, the TEA2262 features the following functions :

- Power supply start-up (with soft-start)
- PWM generator
- Direct power transistor drive (±1A)
- Safety functions : pulse by pulse current limitation, output power limitation, over and under voltage lock-out.

S.M.P.S. OPERATING DESCRIPTION

Starting Mode - Stand By Mode

Power for circuit supply is taken from the mains through a high value resistor before starting. As long as V_{CC} of the TEA2262 is below V_{CC} start, the quiescent current is very low (typically 0.5mA) and the electrolytic capacitor across V_{CC} is linearly charged. When V_{CC} reaches V_{CC} start (typically 11.8V), the circuit starts, generating output pulses with a soft-starting. Then the SMPS goes into the stand-by mode and the output voltage is a percentage of the nominal output voltage (eg. 80%).

During starting phase, in order to avoid transformer magnetization (specially at high frequency), the frequency oscillator is divided by four.

At switch-on, C_0 charging current is divided by four. It recover its normal value when the voltage on soft-start capacitor reach 2.5V.

The current also recover its standard value when the soft-start capacitor is discharged because of a burst operating mode (starting in stand-by).

In other words, the charging current will become and stay at its normal value, as soon as one of the following events occurs :

- V_{C1} rearch 2.5V
- C_1 is discharged by burst operating mode

For this the TEA2262 contains all the functions required for primary mode regulation : a fixed frequency oscillator, a voltage reference, an error amplifier and a pulse width modulator (PWM).

For transmission of low power with a good efficiency in stand-by, an automatic burst generation system is used, in order to avoid audible noise.

Normal Mode (secondary regulation)

The normal operating of the TV set is obtained by sending to the TEA2262 regulation pulses generated by a regulator located in the secondary side of the power supply (TEA5170 for example).

This architecture uses the "Master-slave Concept", advantages of which are now well-known especially the very high efficiency in stand-by mode, and the accurate regulation in normal mode.

Stand-by mode or normal mode are obtained by supplying or not the secondary regulator. This can be ordonnered for exemple by a microprocessor in relation with the remote control unit.

Regulation pulses are applied to the TEA2262 through a small pulse-transformer to the IN input (pin 2). This input is sensitive to positive square pulses. The typical threshold of this input is 0.85V.

The frequency of pulses coming from the secondary regulator can be lower or higher than the frequency of the starting oscillator.

The TEA2262 has no soft-starting system when it receives pulses from the secondary. The soft-starting has to be located in the secondary regulator.

Due to the principle of the primary regulation, pulses generated by the starting system automatically disappear when the voltage delivered by the SMPS increases.

Stand-by Mode - Normal Mode Transition

During the transition there are simultaneously pulses coming from the primary and secondary regulators.

These signals are not synchronized and some care has to be taken to ensure the safety of the switching power transistor.

A very sure and simple way consist in checking the transformer demagnetization state.

- A primary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the secondary regulator.
- A secondary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the primary regulator.

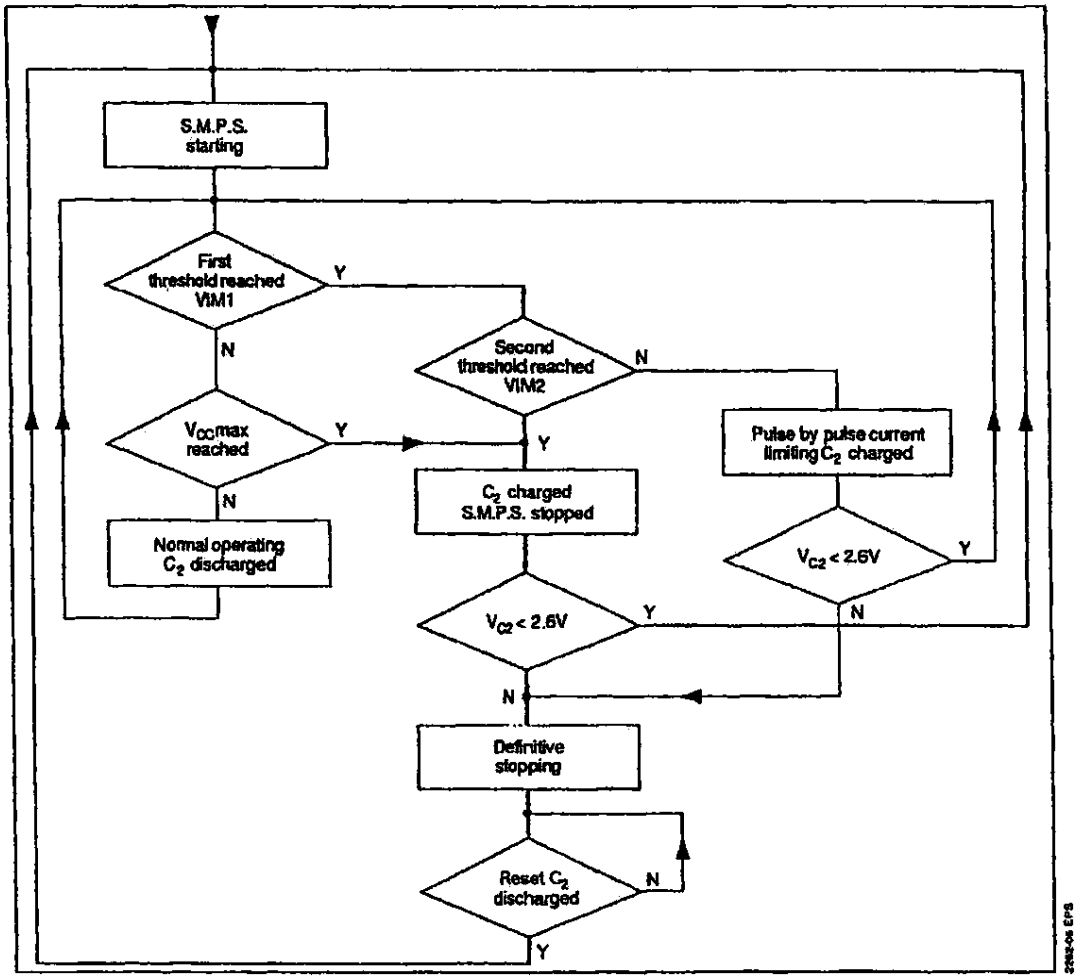
With this arrangement the switching safety area of the power transistor is respected and there is no risk of transformer magnetization.

The magnetization state of the transformer is checked by sensing the voltage across a winding of the transformer (generally the same which supplies the TEA2262). This is made by connecting a resistor between this winding and the demagnetization sensing input of the circuit (pin 1).

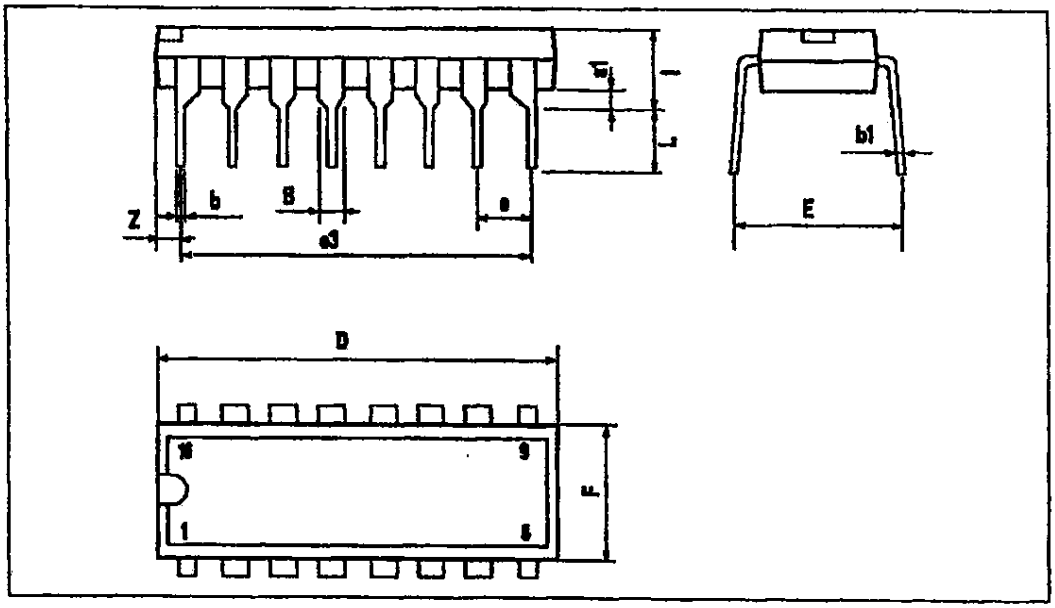
SECURITY FUNCTIONS (see flow-chart below)

- **Undervoltage detection.** This protection works in association with the starting device "V_{CC} switch" (see paragraph Starting-mode - standby mode). If V_{CC} is lower than V_{CC}stop (typically 8.5V) output pulses are inhibited, in order to avoid wrong operation of the power supply or bad power transistor drive.
- **Overvoltage detection.** If V_{CC} exceeds V_{CC}max (typically 15.7V) output pulses are inhibited and the external capacitor C_2 is charged as long as V_{CC} is higher than V_{CC} stop. Restarting of the power supply is obtained by reducing V_{CC} below V_{CC}stop except if the voltage across C_2 reaches V_{C2} (typically 2.55V) (refer to "Restart of the power supply" paragraph). In this last case, the circuit is definitively stopped.
- **Current limitation of the power transistor.** The current is measured by a shunt resistor. A double threshold system is used :
  - When the first threshold (V_{IM1}) is reached, the conduction of the power transistor is stopped until the end of the period : a new conduction signal is needed to obtain conduction again.
  - Furthermore as long as the first threshold is reached (it means during several periods), an external capacitor C_2 is charged. When the voltage across the capacitor reaches V_{C2} (typically 2.55V) the output is inhibited. This is called the "repetitive overload protection". If the overload diseappears before V_{C2} is reached, C_2 is discharged, so transient overloads are tolerated.
  - Second current limitation threshold (V_{IM2}). When this threshold is reached the output of the circuit is immediatly inhibited. This protection is helpfull in case of hard overload for example to avoid the magnetization of the transformer.
- **Restart of the power supply.** After stopping due to V_{IM2}, V_{CC}Max or V_{CC}stop triggering, restart of the power supply can be obtained by the normal operating of the "V_{CC} switch" V_{CC} switch sequency from V_{CC}stop to V_{CC}start . After stopping due to V_{C2} threshold reaching, the circuit is definitively stopped. In this case it is necessary to reduce V_{CC} below approximately 5V to reset the circuit. From a practical point of view, it means that the power supply has to be temporarily disconnected from any power source to get the restart.

SECURITY FLOW-CHART



PACKAGE MECHANICAL DATA
16 PINS - PLASTIC DIP



PM-DIP16.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

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EXHIBIT 2

REDACTED

EXHIBIT 3

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EXHIBIT 4

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EXHIBIT 5

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EXHIBIT 6

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EXHIBIT 7

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EXHIBIT 8

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EXHIBIT 9

United States Patent [19]

Beasom

[11] **Patent Number: 4,823,173**

[45] **Date of Patent: Apr. 18, 1989**

[54] **HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION**

[75] Inventor: James D. Beasom, Melbourne Village, Fla.

[73] Assignee: Harris Corporation, Melbourne, Fla.

[21] Appl. No.: 831,384

[22] Filed: Jan. 7, 1986

[51] Int. Cl.[4] H01L 29/80

[52] U.S. Cl. 357/22; 357/23.8; 357/35

[58] Field of Search ..... 357/23.8, 22 E, 22 F, 357/22 G, 35

[56] **References Cited**

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OTHER PUBLICATIONS

H. Vaes et al., "High-Voltage, High Current Lateral Devices", 1980 IEDM Conf. Proc., Dec. 8–10, 1980, pp. 87–90.

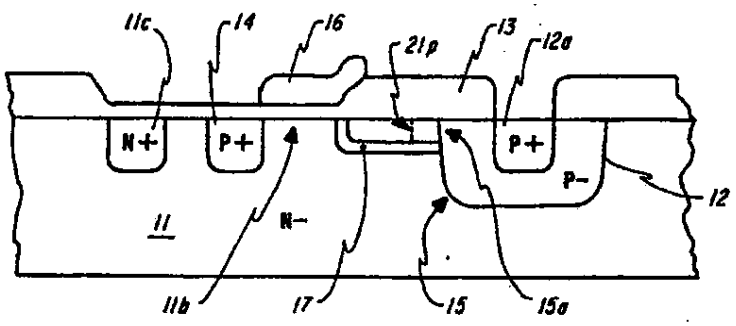
Primary Examiner—Joseph E. Clawson, Jr.

Attorney, Agent, or Firm—William A. Troner; Charles C. Krawczyk

[57] **ABSTRACT**

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

19 Claims, 3 Drawing Sheets



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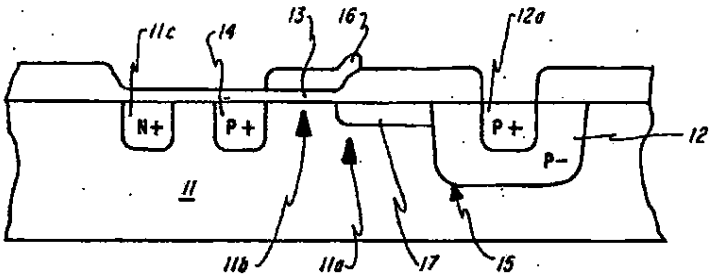

FIG. 1

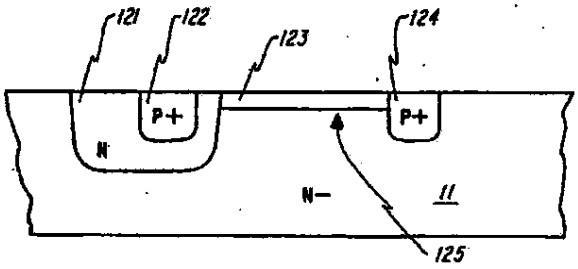

FIG. 2

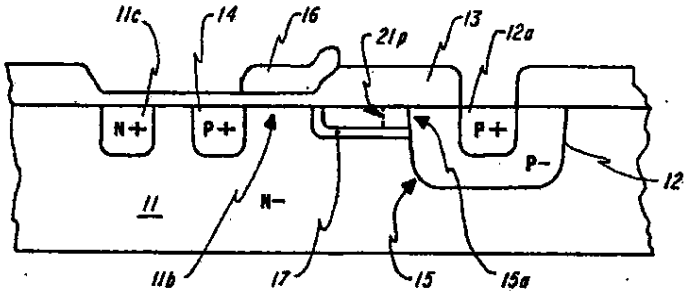

FIG. 3

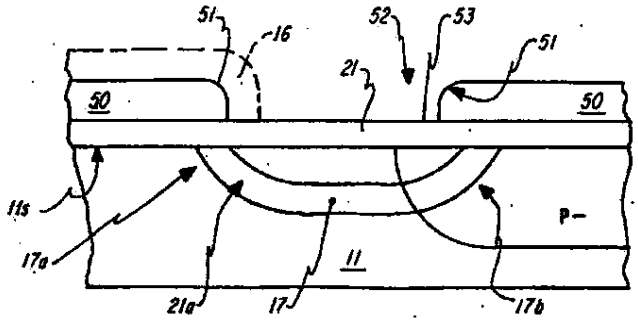

FIG. 4

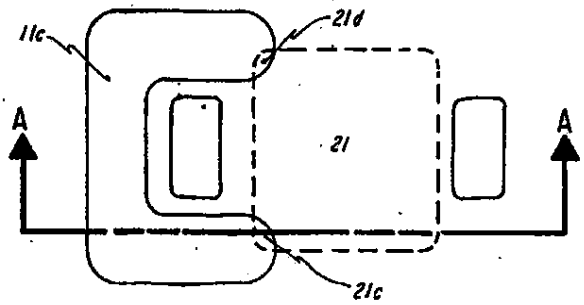

FIG. 5a

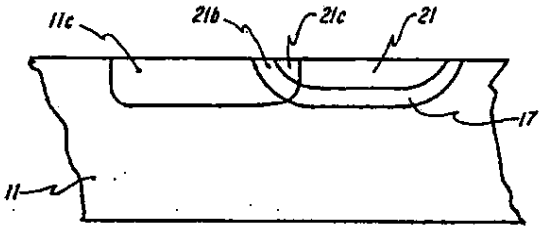

FIG. 5b

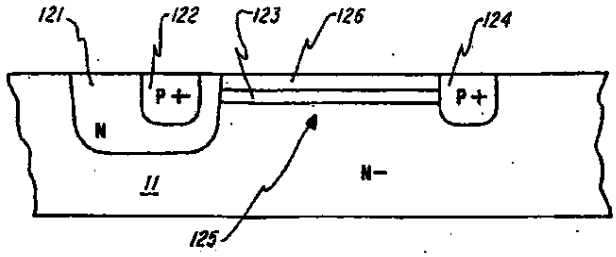

FIG. 6

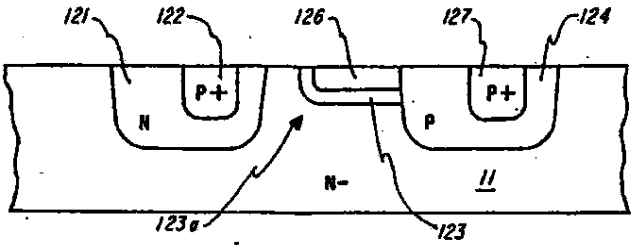

FIG. 7

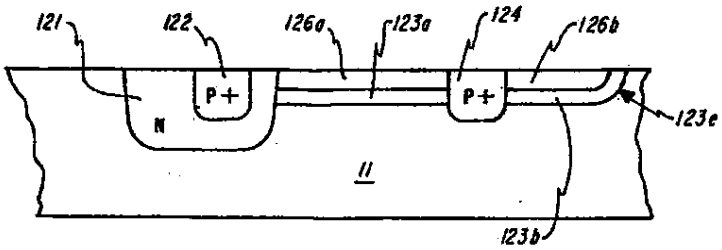

FIG. 8

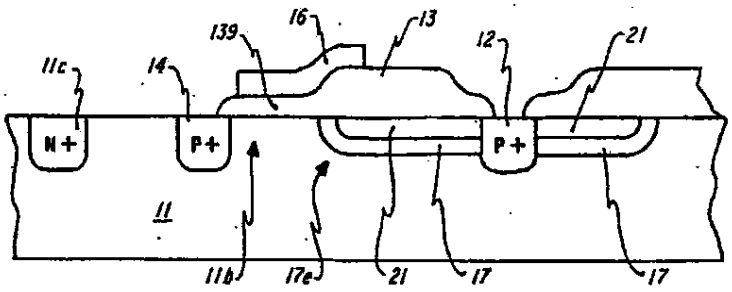

FIG. 9

HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N^{31} substrate 11 and is located so as to lie adjacent the P^- drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12_a and body contact 11_c are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17 serves as a JFET channel with the portion 11_d of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel to body depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also, the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. 2 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. 2, an N^- substrate 11, has an N type emitter shield 121 formed therein and P^+ emitter 122 and collector 124 located as shown. Additionally, a P^- drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In this device, the total collector resistance is equal to the sum of the resistance across the drift region 125 plus the resistance of the P^+ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore providing improved frequency response.

At high base collector voltages the drift region, 123, depletes by JFET action with the N-base, 11, and N

shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section of a known MOS device having typical ON resistance.

FIG. 2 is a cross section of a known bipolar transistor having typical collector resistance.

FIG. 3 is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. 4 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. 5*a* and 5*b* are respectively a top view and is a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. 6 is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. 7 is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. 8 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. 9 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. 3 shows an MOS device where P^+ drain contact $12a$ is formed in P^- type drain 12, P^+ source 14 is formed in the N^- body 11 and N^+ body contact 11_c is provided in the N^- body 11. The MOS channel region 11_b is in the N^- body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_s of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the drain body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any non-depleted portion of the top gate does not result in a breakdown of the top

gate to drift region junction. Proper doping of the top gate will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of FIG. 3 provides reduced ON resistance in the JFET channel relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body to drain breakdown. This is possible because of the provision of the top gate 21. The top gate to channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, results in the reduction in channel resistance. It is posible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel change. Thus, for a drift region having a doping of 1×10^{12} boron atoms per square centimeter over the drift region surface in a bottom gate arrangement, the present invention will permit 2×10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body to drain voltage of less than the breakdown voltage of the top gate to drain junction 15_a. Since top gate 21 is connected to body 11, the voltage at the top gate to drain junction 15_a will equal the voltage of the body to drain junction 15 voltage and the top gate to drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally, the top gate 21 should totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 17 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also desirable to insure that the channel of the JFET drift region contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 4 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially effected by the oxide 53 due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and because of the graduated thickness of the implant mask 50 (along the edge 51) the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion implanted into the drift region using the implant mask 50 but at an energy level which results in a shallower ion penetration. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method a diffusion process can be used to bring the JFET channel into contact with the surface 11_s of body 11, and hence insure that the JFET channel will contact the inversion layer MOS surface channel. The lateral drift region 17 and top gate 21 are diffused into the body 11 after initial introduction by ion implant. The doping levels and diffusion times are chosen such that the extremity 17_a of drift region 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region and top gate may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in FIG. 4 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate while the top gate may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in FIG. 5_a which shows the overlapping of the top gate 21 and the body contact 11_c at overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17 as shown in FIG. 5_b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

FIG. 5_b shows a cross section of the structure of FIG. 5_a taken along dashed line A—A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body

contact 11_c. Thus, so long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. 2 may be improved by providing an N type top gate 126 as shown in FIG. 6. In this arrangement the top gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate to drift region depletion layer facilitates pinch-off of the drift region. However, as the base 11 becomes more negative the top gate 126 contributes additional surface exposure to the drift region 123 resulting in lower collector resistance.

FIG. 7 shows an improvement over the arrangement shown in FIG. 6. In FIG. 7 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in FIG. 7 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in FIG. 6 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base to collector breakdown voltage for a PNP device is shown in FIG. 8. In addition to the provision of the N type top gate 126_a over the P− drift region 123_a, the top gate and drift region are enlarged to surround the collector 124 and a curved edge 123_e is provided at the periphery of the enlarged portion 123_b of the drift region. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P+ emitter 122 is formed in the N+ type emitter shield.

FIG. 9 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. 8. For the MOS device, the P+ drain 12 is surrounded by the P− drift region 17 and N type top gate 21. Around the entire periphery of the drift region there is a curved portion 17_d which rounds up to the surface of the N− substrate 11 to insure that the JFET channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source 14 and N+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in FIG. 8 and FIG. 9, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. 8 and drain in FIG. 9 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

1. In a semiconductor device of the type including a lateral drift region of a first conductivity type formed in a body region, said drift region serving as a JFET channel, the improvement comprising:
   a top gate of a semiconductor material electrically connected to said body region and having a second conductivity type over said drift region to cause depletion of said drift region rom the top upon application of a reverse bias voltage to said device,
   wherein said top gate laterally abutts a device region to form a junction and has a surface area doping density such that said top gate becomes totally depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction, and
   wherein said top gate has a surface are a doping density such that it becomes totally depleted at a reverse bias voltage less than the reverse bias voltage at which said drift region becomes depleted.

2. A semiconductor device as claim 1 wherein said drift region as a tapered peripheral edge.

3. A semiconductor device as claimed in claim 2 wherein said top gate has a lateral expanse bounded by said drift region.

4. A semiconductor device as claimed in claim 3 wherein said top gate has a tapered peripheral edge.

5. A semicondcutor device comprising:
   a semiconductor body of a first conductivity type;
   a first device region of a second conductivity type formed in said body;
   a second device region of said second conductivity type formed in said body and separated from said first device region;
   a drift region of said second conductivity type formed in said body between said first and second device regions, separated from said second device region by a separation zone and in contact with said first device region, said drift region having a first side adjacent said body;
   a top gate of said first conductivity type adjacent a substantial portion of a second side of said drift region and electrically connected to said body;

wherein said top gate and semiconductor body operable as a top and bottom gate respectively of a JFET channel formed by said drift region;

said top gate having a surface area doping density such that it becomes totally depleted at a body to first device region voltage below the voltage at which the body to drift region depletion layer in said first side of said drift region reaches the top gate to drift region depletion layer in said second side of said drift region.

6. A semiconductor device as claimed in claim 5 wherein said first device region is a drain of a lateral drift region MOS device;

said semiconductor device further comprising an MOS gate located over said separation zone and overlapping a portion of said drift region.

7. A semiconductor device as claimed in claim 5 wherein said first device region is a collector of a lateral bipolar transistor and wherein said separation zone comprises an emitter shield region of said first conductivity type.

8. A semiconductor device as claimed in claim 5 wherein said drift region and top gate are in contact with said first device region about the entire periphery of said first device region.

9. A lateral MOS structure comprising a semiconductor body of a first conductivity type, source and drain regions of a second conductivity type forming respective source and drain junctions with said body, and a drift region of said second conductivity type, said drift region forming a JFET channel in said body controlled by said semiconductor body which body operates as a JFET gate such that upon application of a reverse bias to said body to drain junction said drift regions becomes depleted, and

a top gate of said first conductivity type formed in said drift region and being electrically connected to said body, said top gate having a surface area doping density such that it becomes totally depleted below a body to drain voltage at which said drift region becomes depleted.

10. A lateral MOS structure as claimed in claim 9 wherein:

said top gate is laterally spaced from said drain.

11. A lateral MOS structure as claimed in claim 9 wherein:

a body contact of said first conductivity type is formed in said body and said top gate overlaps said body contact, said body contact having an impurity concentration higher than the impurity concentration of said drift region.

12. A lateral MOS structure as claimed in claim 9 wherein:

said drift region and said top gate extend laterally around the entire surface intersection of the drain to body junction to reduce the surface field and thereby increase breakdown voltage of the drain to body junction.

13. A lateral MOS structure as claimed in claim 9 wherein:

said top gate totally depletes below a body to drain voltage at which said drift region totally depletes.

14. A lateral MOS structure as claimed in claim 9 wherein:

said top gate is formed by an ion implant, and said top gate has a tapered peripheral edge.

15. A lateral MOS structure as claimed in claim 14 wherein:

said drift region is formed by an ion implant and said drift region has a tapered peripheral edge.

16. A diode structure comprising:

a first semiconductor body of a first conductivity type contained within a semiconductor region of a second conductivity type and forming a diode junction therewith, said semiconductor region having a first dopant concentration,

a second body of said first conductivity type contained within said semiconductor region and having a second dopant concentration greater than said first dopant concentration, said second body surrounding the lateral perimeter of said first body and abutting said first body;

said second body forming a JFET channel controlled by said semiconductor region which region operates as a JFET gate such that upon application of a reverse bias to said region to first body junction said second body becomes depleted, and

a top gate of said second conductivity type formed within said second body and being electrically connected to said first semiconductor region, said top gate having a dopant concentration such that upon application of said reverse bias, said top gate becomes totally depleted before said second body becomes depleted.

17. In a diode structure as claimed in claim 16, the improvement comprising:

a tapered peripheral edge for said top gate.

18. In a diode structure as claimed in claim 17, the improvement comprising:

forming said tapered peripheral edge by implanting said top gate using an implant mask with a tapered edge.

19. In a diode structure as claimed in claim 16, the improvement comprising:

forming a tapered peripheral edge for said second body by implanting said second body using an implant mask with a tapered edge.

* * * * *

EXHIBIT 10

REGULAR UTILITY

Form PTO-436 (Rev. 8/78)

4823173

SERIAL NUMBER (series of 1979)	PATENT DATE	PATENT NUMBER
831384	APR 18 1989	4823173

SERIAL NUMBER	FILING DATE	CLASS	SUBCLASS	GROUP ART UNIT	EXAMINER
06/831,384	01/07/86	~~429~~ 357	22	~~151~~ 253 JRC	Clawson

APPLICANTS

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CONTINUING DATA******** NONE
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FOREIGN/PCT APPLICATIONS******** NONE
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Foreign priority claimed 35 USC 119 conditions met	Verified and Acknowledged	Examiner's Initials	AS FILED	STATE OR COUNTRY	SHEETS DRWGS	TOTAL CLAIMS	INDEP CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO
☐ yes ☒ no ☐ yes ☐ no				FL	5	25	3	$ 434.00	SE-395

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TITLE

HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION

U.S. DEPT of COMM.-Pat. & TM Office — PTO-436L (rev 10-78)

PARTS OF APPLICATION FILED SEPARATELY

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20162	02/26/96	831384		08-0870	020	101	340.00CH
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831384

Case SE-395

APPLICATION TRANSMITTAL LETTER

IN THE UNITED STATES PATENT
AND TRADEMARK OFFICE

THE COMMISSIONER OF PATENTS AND TRADEMARKS

WASHINGTON, D.C. 20231

SIR: Transmitted herewith for filing are the following parts of the patent application of Inventor(s):

James D. Beasom

For: A High Voltage Lateral MOS Structure

Serial No.:
Filed:

[X] specification and claim(s)

[5] sheet of drawing.

[X] An assignment of the invention to HARRIS CORPORATION.

[ ] A certified copy of a _____ application.

[ ] Associate Power of Attorney.

[X] Declaration and Power of Attorney.

00010

Claims as filed

	Number filed	Number extra	Rate	Fee
Total claims	25	- 20= 5	$10.00	$ 50.00
Independent claims	4	- 3= 1	$30.00	$30.00
		Basic Filing Fee:		$300.00
		Total Filing Fee:		$380.00

[X] Please charge my Deposit Account No. 08-0870 in the amount of $ 380.00 . A duplicate copy of this sheet is enclosed.

[X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 08-0870 . A duplicate copy of this sheet is enclosed.

[ ] A check in the amount of _____ to cover the filing fee is enclosed.

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Sincerely,

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FCS1688781

831384

Attorney Docket SE-395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR: James D. BEASOM

INVENTION: A HIGH VOLTAGE LATERAL MOS STRUCTURE

SPECIFICATION

To All Whom It May Concern:

Be it known that I, James D. Beasom, citizen of the United States of America, residing at 506 S. Wildwood ~~Drive~~ Lane, Melbourne Village, Florida, 32904, have invented certain new and useful improvements in

A HIGH VOLTAGE LATERAL MOS STRUCTURE

of which the following is a specification.

Attorney Docket SE-395

FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, Fig. 1 illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain body junction 15 as the basic high voltage junction of the device. The drift region 17 is a P region along the top surface of the N^- substrate 11 and is located so as to lie adjacent the P^- drain region 12. The drift region 17 is used to connect the high voltage drain 12 to the gate 16 and source 14. The two contacts, drain contact 12_a and body contact 11_c are shown for completeness. In the operation of this circuit, the gate 16 and source 14 never assume large voltages relative to the body 11. The drift region 17 serves as a JFET channel with the portion 11_a of body region 11 underlying the channel acting as a JFET gate. The JFET channel 17 is designed to totally deplete when the drain 12 is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel to body

depletion layer. This design preserves the effective high breakdown voltage of drain body junction 15. Also, the source 14 and gate 16 (over the gate oxide 13) are safely shielded from the high drain body voltage by the pinched off JFET channel 17.

The resistance of the lateral drift region JFET channel 17 is in series with the resistance of the MOS channel 11_b, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

Fig. 2 shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in Fig. 7 of U.S. Patent NO. 4,283,236 issued August 11, 1981. Referring to Fig. 2, an N^- substrate 11, has an N type emitter shield 121 formed therein and P^+ emitter 122 and collector 124 located as shown. Additionally, a P^- drift region 123 is provided along the surface of the substrate between the collector 124 and the emitter shield 121. In this device, the total collector resistance is equal to the sum of the resistance across the drift

region 125 plus the resistance of the P^+ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, 121, so that the base width is just that small distance between the adjacent edges of the emitter, 121, and the drift region, therefore providing improved frequency response.

At high base collector voltages the drift region, 123, depletes by JFET action with the N-base, 11, and N shield, 121, which is part of the base, acting as gate before critical field is reached just as for the MOS of Figure 1. This preserves the high breakdown of the structure.

SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross section of a known MOS device having typical ON resistance.

Fig. 2 is a cross section of a known bipolar transistor having typical collector resistance.

Fig. 3 is a cross section of an MOS device including the improved drift region and top gate of the invention.

Fig. 4 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

Figs. 5a and 5b are respectively a top view and is a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

Fig. 6 is a cross section of a bipolar device made in accordance with one aspect of the invention.

Fig. 7 is a cross section of a bipolar device made in accordance with another aspect of the invention.

Fig. 8 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

Fig. 9 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. Fig. 3 shows an MOS device where P^+ drain contact 12_a is formed in P^- type drain 12, P^+ source 14 is formed in the N^- body 11 and N^+ body contact 11_c is provided in the N^- body 11. The MOS channel region 11_b is in the N^- body 11 below the MOS gate 16. The N type top gate 21 is provided along the surface 11_s of the body 11 above the P type drift region 17 which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate 21 and drift region 17 extend to the drain body junction 15 and preferably terminate at the junction 15. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction 15. In this case care should be taken to insure that any non-depleted portion of the top gate does not result in a breakdown of the top gate to drift region junction. Proper doping of the top gate will generally be a sufficient preventative step. Dashed line 21_p designates the peripheral edge of top gate 21 in an embodiment where the top gate does not extend all the way to the junction 15.

The structure of Figure 3 provides reduced ON resistance in the JFET channel relative to the prior art lateral drift MOS device as shown in Fig.

1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body to drain breakdown. This is possible because of the provision of the top gate 21. The top gate to channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, results in the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel change. Thus, for a drift region having a doping of 1 x 10^{12} boron atoms per square centimeter over the drift region surface in a bottom gate arrangement, the present invention will permit 2 x 10^{12} boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate 21 must be designed differently than an ordinary JFET gate. Top gate 21 should become totally depleted at a body to drain voltage of less than the breakdown voltage of the top gate to drain junction 15_a. Since top gate 21 is connected to body 11, the voltage at the top gate to drain junction 15_a will equal the voltage of the body to drain junction 15 voltage and the top gate to drain breakdown voltage should be greater than the voltage at which top gate 21 becomes totally depleted. Additionally,

the top gate 21 should totally deplete before the body 11 to channel 17 depletion layer reaches the top gate 21 to channel 17 depletion layer to thereby assure that a large top gate 17 to drain 12 voltage is not developed by punch-through action from the body 11. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also desirable to insure that the channel of the JFET drift region contacts the inversion layer MOS surface channel. This can be accomplished as shown in Fig. 4 where an implant mask 50 having a tapered edge 51 is provided over the body 11. An implant aperture 52 is provided in mask 50 at the location where the P drift region 17 and top gate 21 are to be formed. The aperture 52 is shown as exposing the protective oxide 53. Ion implantation is not substantially effected by the oxide 53 due to the oxide thickness of only about 0.1-0.2 micrometers, yet the oxide provides surface passivation for the underlying body 11.

The drift region 17 is ion implanted and because of the graduated thickness of the implant mask 50 (along the edge 51) the depth of the implanted drift region 17 is graduated or tapered. In the illustration, a fairly good rounding of the drift region 17 occurs at the peripheral edges or extremities 17_a, 17_b of the region 17. The curved extremity 17_a is of

interest because at this location the channel of the JFET drift region 17 contacts the surface 11_s of body 11 beyond the end 21_a of top gate 21 and is desirably beneath the gate 16 of the MOS device. The top gate 21 may be ion implanted into the drift region using the implant mask 50 but at an energy level which results in a shallower ion penetration. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method a diffusion process can be used to bring the JFET channel into contact with the surface 11_s of body 11, and hence insure that the JFET channel will contact the inversion layer MOS surface channel. The lateral drift region 17 and top gate 21 are diffused into the body 11 after initial introduction by ion implant. The doping levels and diffusion times are chosen such that the extremity 17_a of drift region 17 diffuses beyond the end 21_a of the top gate 21 and so that the end 17_a reaches the surface 11_s of body 11. In practice, this approach can be facilitated by choosing a top gate dopant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region and top gate may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant

mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask 50 illustrated in figure 4 is shown as having thin oxide portion 53 being surrounded by the implant mask 50. If the MOS gate 16 shown in dashed lines were used as a portion of the mask 50, the edge of the drift region and top gate would be self aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate while the top gate may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate 21 will perform as previously described if it is tied to the body 11. Thus, the top gate 21 and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region 17 is widened to overlap with the body contact region 11_c. This is shown in Fig. 5_a which shows the overlapping of the top gate 21 and the body contact 11_c at overlap regions 21_c, 21_d. In order for this arrangement to be effective, it is necessary that the body contact 11_c have a higher dopant concentration than the JFET channel (or drift region) 17 as

shown in Fig. 5_b to insure that the body contact 11_c forms a continuous region horizontally and/or vertically through the JFET channel and to the body region 11 from the top gate, 21.

Figure 5_b shows a cross section of the structure of Figure 5_a taken along dashed line A-A. The body 11 is provided with body contact 11_c which is located such that the top gate 21 and drift region 17 can be conveniently extended to overlap the body contact 11_c. The depth of body contact 11_c may be made greater than the depth of region 17 such that a portion of the body contact 11_c extends below region 17 and provides contact with the body 11. This arrangement provides a contact portion 21_c where the top gate 21 is in contact with body contact 11_c. Thus, so long as the body contact doping concentration in region 21_b is sufficiently high to overcome the opposite doping in region 17, then a good connection of uniform conductivity type will be provided between the top gate 21 and the body 11. It is also noted that the body contact 11_c extends laterally beyond the end of both of the top gate 21 and the drift region 17. The lateral extension of the contact 11_c will also provide a structure which results in a good connection of uniform conductivity type from the top gate 21 to the body 11, again, provided that the doping of body contact 11_c converts region 21_b.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of Fig. 2 may be improved by providing an N type top gate 126 as

shown in Fig. 6. In this arrangement the top gate 126 extends from the collector 124 to the emitter shield 121 along the surface of body 11. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base 11 becomes positive relative to the collector 124, the top gate to drift region depletion layer facilitates pinch-off of the drift region. However, as the base 11 becomes more negative the top gate 126 contributes additional surface exposure to the drift region 123 resulting in lower collector resistance.

Fig. 7 shows an improvement over the arrangement shown in Fig. 6. In Fig. 7 the drift region 123 does not extend all the way over to the emitter shield 121. The curved end 123_a of the drift region 123 contacts the top surface of body 11. It is noted that in this arrangement, the emitter shield 121 may be omitted.

An additional improvement shown in Fig. 7 is the use of a deep diffusion to form the collector 124 resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector 124 shown in Fig. 6 would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact 127 may then be formed simultaneously with the formation of the emitter 122. This improvement in junction breakdown voltage is

equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base to collector breakdown voltage for a PNP device is shown in Fig. 8. In addition to the provision of the N type top gate 126_a over the P^- drift region 123_a, the top gate and drift region are enlarged to surround the collector 124 and a curved edge 123_e is provided at the periphery of the enlarged portion 123_b of the drift region. This enlarged portion is designated by reference numerals 123_b for the drift region and 126_b for the top gate. The collector 124 to base 11 breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate 126_a extends to the emitter shield 121 as does the drift region 123_a. The P^+ emitter 122 is formed in the N^+ type emitter shield.

Fig. 9 illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in Fig. 8. For the MOS device, the P^+ drain 12 is surrounded by the P^- drift region 17 and N type top gate 21. Around the entire periphery of the drift region there is a curved portion 17_e which rounds up to the surface of the N^- substrate 11 to insure that the JFET

channel in the drift region 17 contacts the MOS channel 11_b under the MOS gate 16. The drift region 17 extends outward from the entire perimeter of the drain 12. This arrangement mitigates the breakdown reduction due to junction curvature. The P^+ source 14 and N^+ body contact 11_c are shown as is the dielectric 13 which serves as the gate oxide 13_g beneath the MOS gate 16.

In both the arrangements shown in Fig. 8 and Fig. 9, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in Fig. 8 and drain in Fig. 9 and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

Cm what is claimed is:

Attorney Docket SE-395

WHAT IS CLAIMED IS:

1. In a semiconductor device of the type including a drift region of a first conductivity type, the improvement comprising:

providing a top gate of a second conductivity type over said drift region to cause depletion of said drift region from both top and bottom upon application of a reverse bias voltage to said device.

2. A semiconductor device as claimed in claim 1, wherein said top gate abutts a device region and said top gate becomes depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction.

3. A semiconductor device as claimed in claim 2 wherein said top gate becomes depleted at a reverse bias voltage less then the reverse bias voltage at which said drift region becomes depleted.

4. A semiconductor device as claimed in claim 1 wherein said drift region has a tapered peripheral edge.

5. A semiconductor device as claimed in claim 4 wherein said top gate has a lateral expanse bounded by said drift region.

Attorney Docket SE-395

8. A semiconductor device as claimed in claim 5 wherein said top gate has a tapered peripheral edge.

7. A semiconductor device comprising:

a semiconductor body of a first conductivity type;

a first device region of a second conductivity type formed in said body;

a second device region of said second conductivity type formed in said body and separated from said first device region;

a drift region of said second conductivity type formed in said body between said first and second device regions, separated from said second device region by a separation zone and in contact with said first device region, said drift region having a first side adjacent said body;

a top gate of said first conductivity type adjacent a substantial portion of a second side of said drift region;

said top gate becoming depleted at a body to first device region voltage below the voltage at which the body to drift region depletion layer in said first side of said drift region reaches the top gate to drift region depletion layer in said second side of said drift region.

8. A semiconductor device as claimed in claim 7 wherein said first device region is a drain of a lateral drift region MOS device;

said semiconductor device further comprising an MOS gate located over said separation zone and overlapping a portion of said drift region.

9. A semiconductor device as claimed in claim 7 wherein said first device region is a collector of a lateral bipolar transistor and wherein said separation zone comprises an emitter shield region of said first conductivity type.

10. A semiconductor device as claimed in claim 7 wherein said drift region and top gate are in contact with said first device region about the entire periphery of said first device region.

CLAIM 9

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11. In a lateral MOS structure comprising a semiconductor body of a first conductivity type, source and drain regions of a second conductivity type, and a drift region of said second conductivity type, said drift region forming a JFET channel controlled by said semiconductor body which body operates as a JFET gate such that upon application of a reverse bias to said body to drain junction said drift region becomes depleted, the improvement comprising:

a top gate of said first conductivity type formed over said drift region.

12. A lateral MOS structure as claimed in claim 11 wherein:

said top gate becomes depleted below a body to drain voltage at which the body to channel depletion layer reaches the top gate to channel depletion layer.

13. A lateral MOS structure as claimed in claim 11 wherein:

said drift region is formed in said semiconductor body along a top surface of said semiconductor body and said top gate is formed in said drift region along said top surface such that said drift region is between said top gate and said semiconductor body.

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14. A lateral MOS structure as claimed in ~~claim 13~~ wherein:

said drift region extends from said body to said top gate.

~~15~~ 10. A lateral MOS structure as claimed in claim ~~14~~ 9 wherein:

said top gate is laterally spaced from said drain.

~~16~~ 11. A lateral MOS structure as claimed in claim ~~14~~ 9 wherein:

a body contact of said first conductivity type is formed in said body and said top gate overlaps said body contact, said body contact having an impurity concentration higher than the impurity concentration of said drift region.

~~17~~ 12. A lateral MOS structure as claimed in claim ~~14~~ 9 wherein:

said drift region and said top gate extend laterally around the entire surface intersection of the drain to body junction to reduce the surface field and thereby increase breakdown voltage of the drain to body junction.

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13. A lateral MOS structure as claimed in claim 12 wherein:

said top gate totally depletes below a body to drain voltage at which said drift region totally depletes.

14. A lateral MOS structure as claimed in claim 12 wherein:

said top gate is formed by an ion implant, and said top gate has a tapered peripheral edge.

15. A lateral MOS structure as claimed in claim 14 wherein:

said drift region is formed by an ion implant and said drift region has a tapered peripheral edge.

21. A lateral MOS structure as claimed in claim 12 wherein:

said top gate becomes depleted at a body to drain voltage below the breakdown voltage of the junction of said top gate to said drain region.

22. In a diode structure comprising a first semiconductor body of a first conductivity type in a semiconductor region of a second conductivity type, and a second body of said second conductivity type completely surrounding the perimeter of said first body and adjacent thereto;

said second body forming a JFET channel controlled by said semiconductor region which region operates as a JFET gate such that upon application of a reverse bias to said region to first body junction said second body becomes depleted, the improvement comprising:

a top gate of said second conductivity type formed over said second body.

23. In a diode structure as claimed in claim 22, the improvement comprising:

a tapered peripheral edge for said top gate.

24. In a diode structure as claimed in claim 23, the improvement comprising:

forming said tapered peripheral edge by implanting said top gate using an implant mask with a tapered edge.

19 16
~~25.~~ In a diode structure as claimed in claim ~~22~~, the improvement comprising:

forming a tapered peripheral edge for said second body by implanting said second body using an implant mask with a tapered edge.

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end

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ABSTRACT OF THE DISCLOSURE

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

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Attorney's Docket No. _____

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT OR CIP APPLICATION)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A High Voltage Lateral MOS Structure

the specification of which: *(complete (a), (b) or (c) for type of application)*

REGULAR OR DESIGN APPLICATION

(a) ☒ is attached hereto.

(b) ☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (*if applicable*).

PCT FILED APPLICATION ENTERING NATIONAL STAGE

(c) ☐ was described and claimed in International Application No. _____ filed on _____ and as amended on _____ (*if any*).

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

☐ In compliance with this duty there is attached an information disclosure statement. 37 CFR 1.97.

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

(complete (d) or (e))

(d) ☒ no such applications have been filed.

(e) ☐ such applications have been filed as follows

EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION

Country	Application No.	Date of filing (day, month, year)	Date of issue (day, month, year)	Priority Claimed
				☐ YES NO ☐
				☐ YES NO ☐
				☐ YES NO ☐

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO SAID APPLICATION

CONTINUATION-IN-PART

(complete this part only if this is a continuation-in-part application)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (Filing Date) (Status) (patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status) (patented, pending, abandoned)

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (*List name and registration number*)

Thomas N. Twomey, Reg. No. 28,910 and Les J. Hart, Reg. No. 25,462, both having a mailing address of P.O. Box 883, Melbourne, Fl 32901-0101, and Charles C. Krawczyk, Reg. No. 22,453 having a mailing address of 1025 West Nasa Blvd., Melbourne, Fl 32919.

SEND CORRESPONDENCE TO
Thomas N. Twomey
Sector Patent Counsel
Harris Semiconductor
PO Box 883
Melbourne, FL 32901-0101

DIRECT TELEPHONE CALLS TO: (name and telephone number)
305-729-4508

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor James D. Beason

Inventor's signature James D. Beason

Date 2/4/86 Country of Citizenship U. S. A.

Residence 506 S. Wildwood ~~Drive~~ LANE, Melbourne Village, Florida 32904

Post Office Address 506 S. Wildwood ~~Drive~~ LANE, Melbourne Village, FL 32904

Full name of second joint inventor, if any

Inventor's signature

Date Country of Citizenship

Residence

Post Office Address

CHECK PROPER BOX(ES) FOR ANY ADDED PAGE(S) FORMING A PART OF THIS DECLARATION

☐ Signature for third and subsequent joint inventors. Number of pages added _____

☐ Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. Number of pages added _____

☐ Signature for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. Number of pages added _____

FIGURE 1

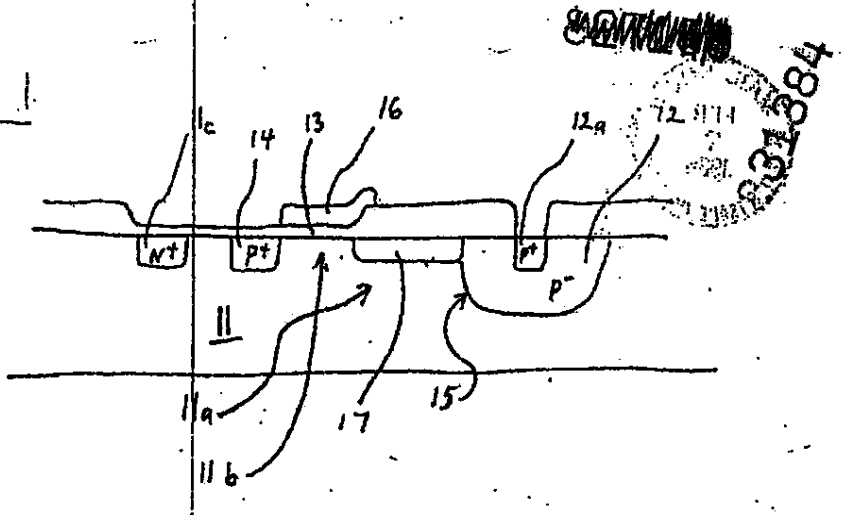

FIGURE 2

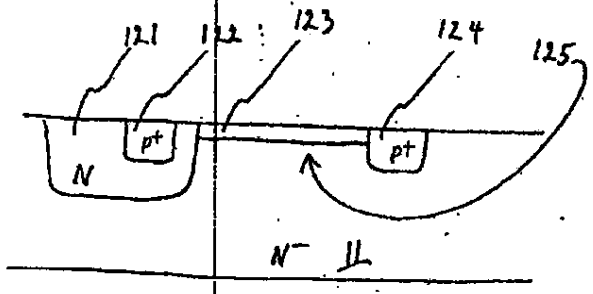

FIGURE 3

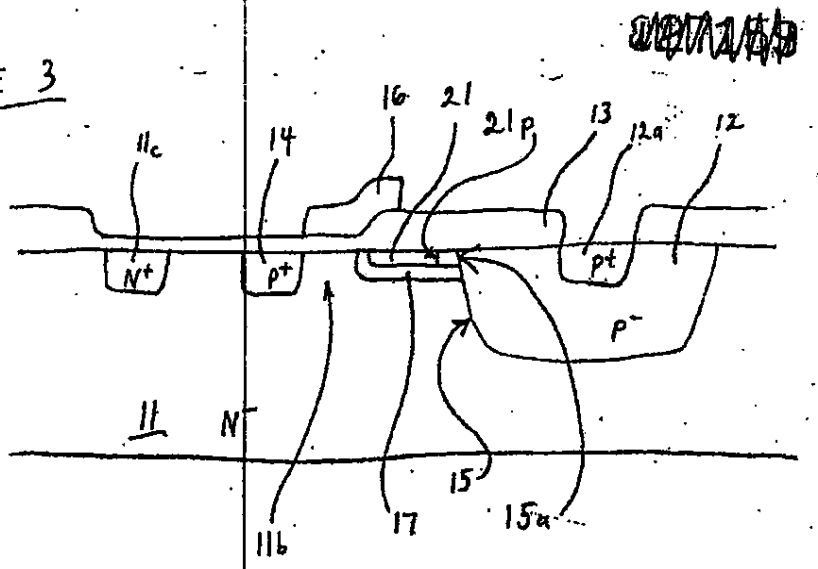

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FIGURE 4

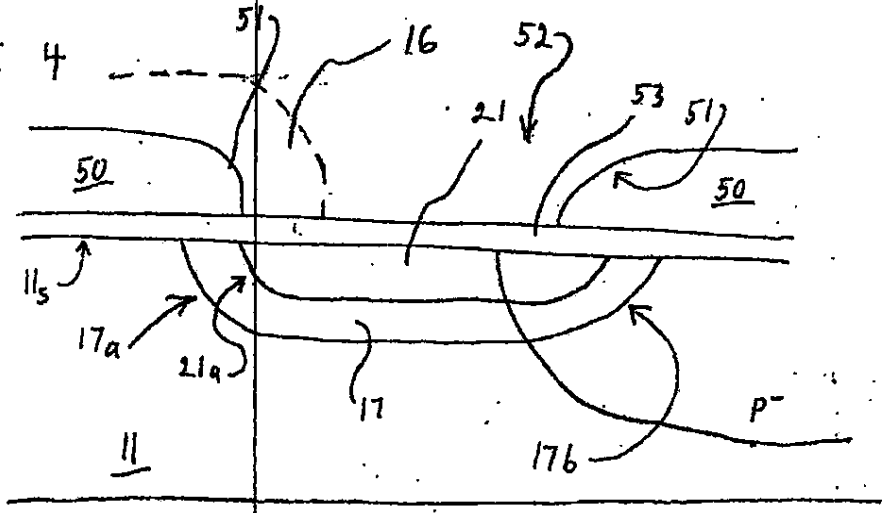

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FIGURE 5a

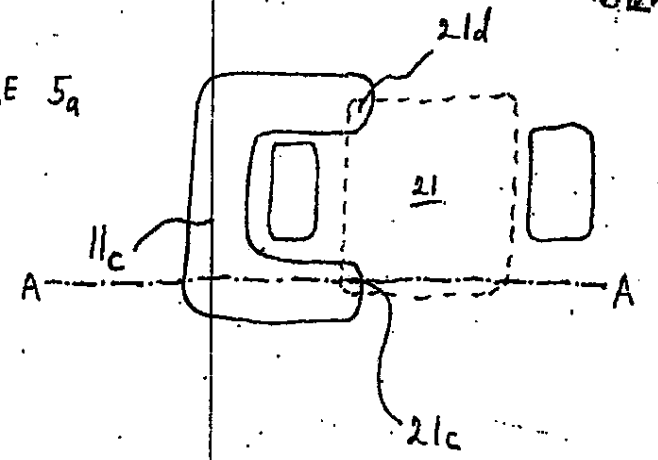

FIGURE 5b

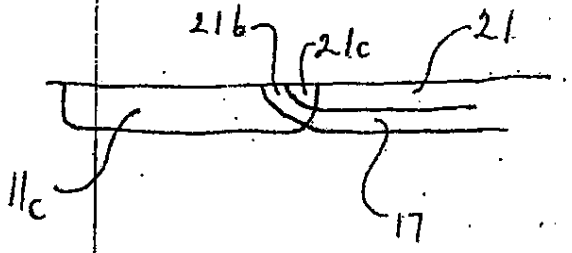

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FIGURE 6

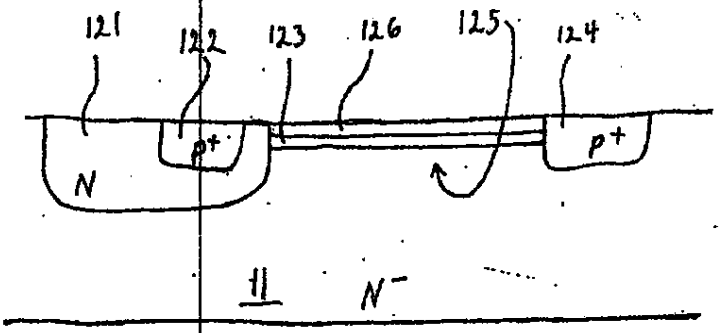

FIGURE 7

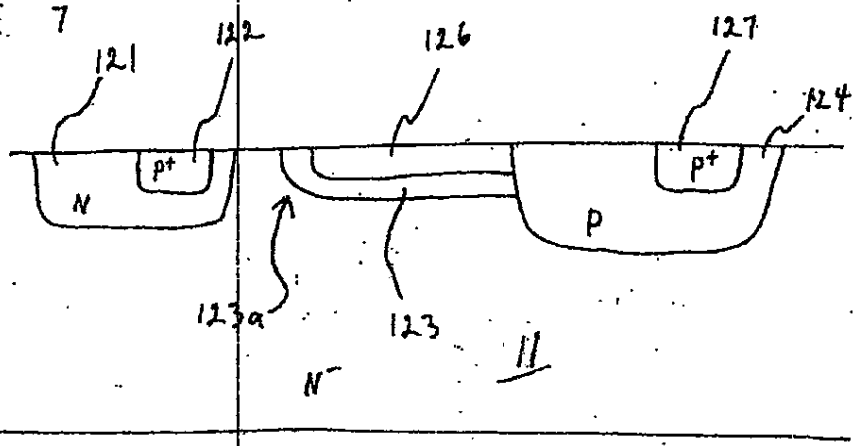

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FIGURE 8

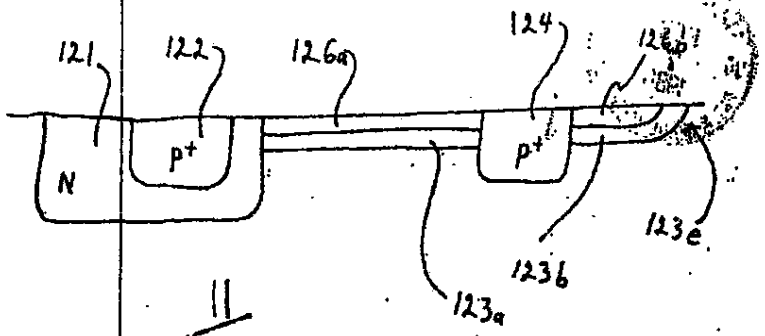

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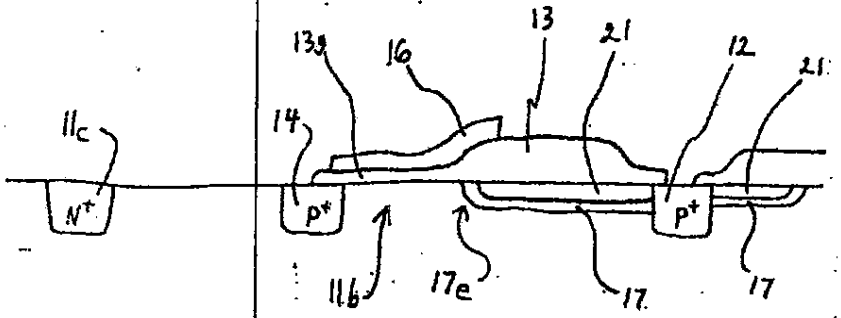
FIGURE 9



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Print Of Drawing
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FIGURE 1

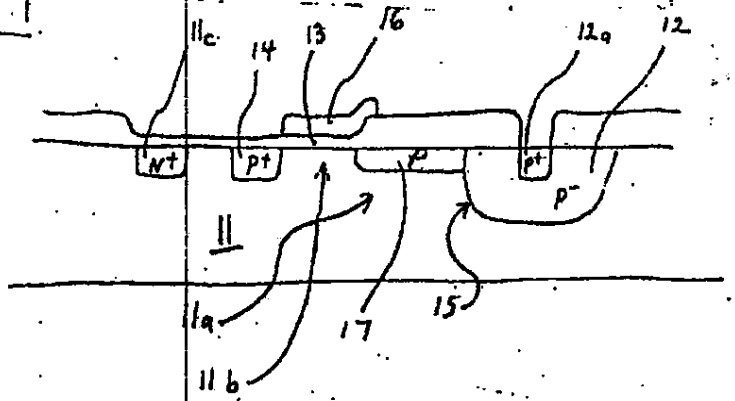

FIGURE 2

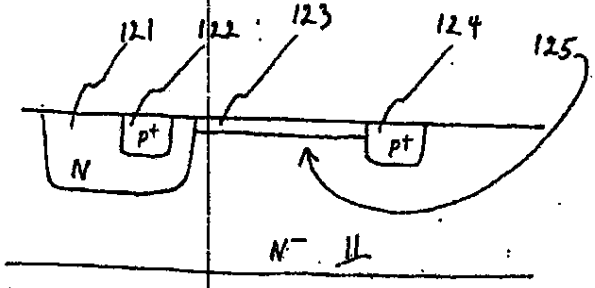

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FIGURE 3

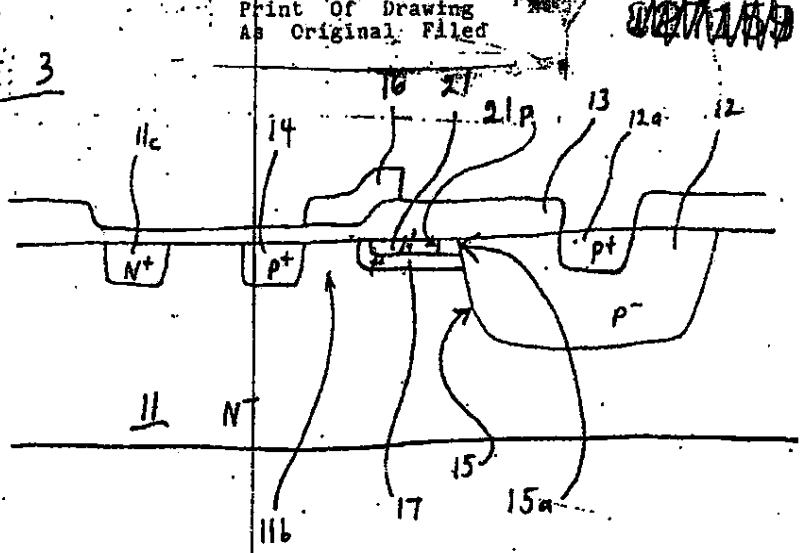
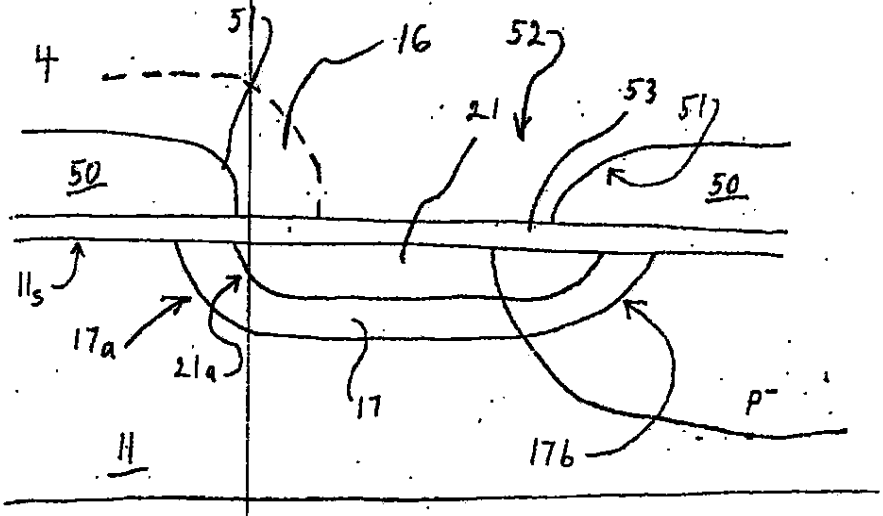


FIGURE 4



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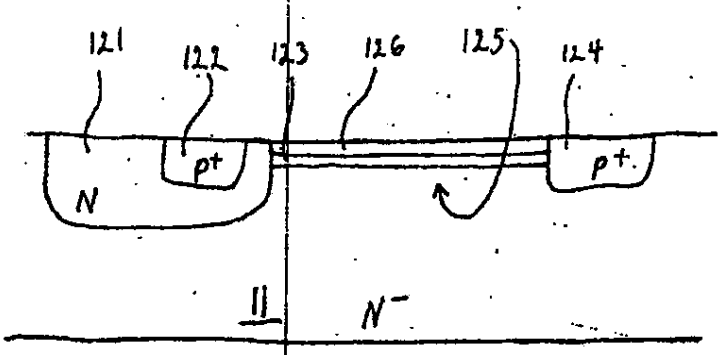
IGURE 6



GURE 7

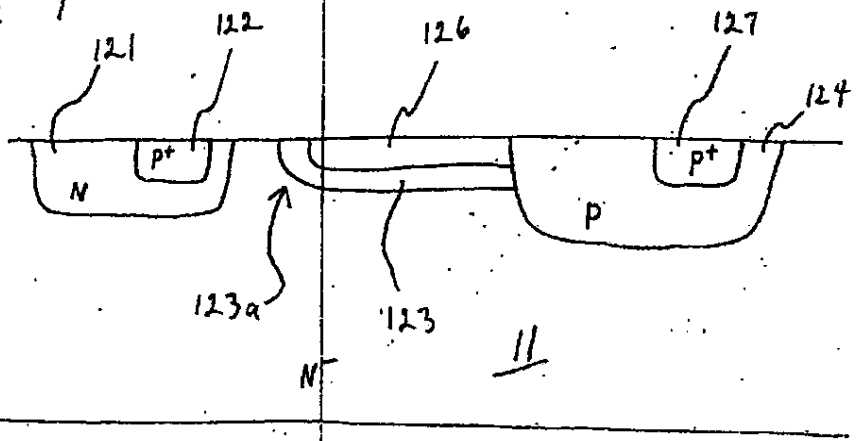


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FIGURE 8

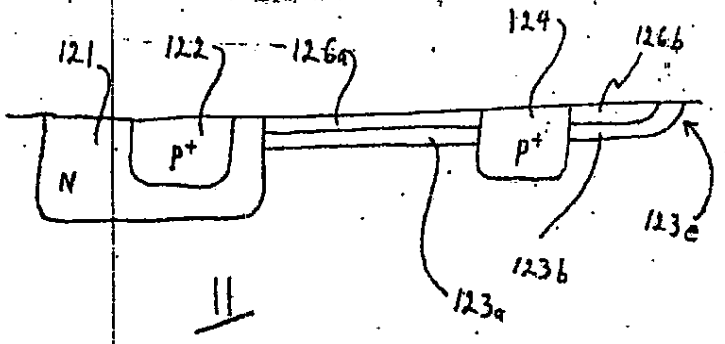

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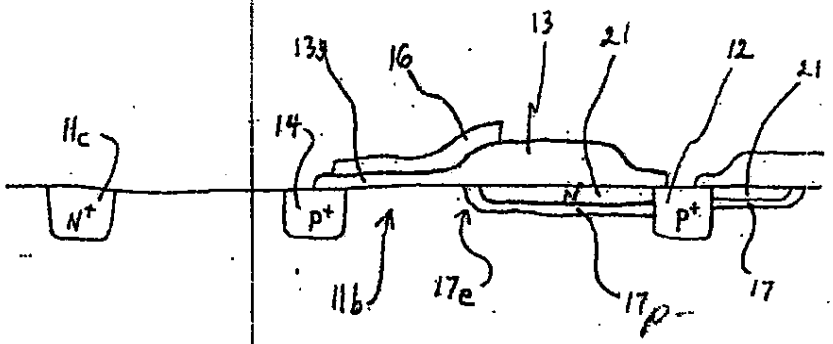
FIGURE 9



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Patent and Trademark Office

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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/831,384	01/07/96	BEASOM	[illegible]

THOMAS H. TWOMEY
SECTOR PATENT COUNSEL
HARRIS SEMICONDUCTOR
P. O. BOX 883
MELBOURNE, FL 32901-0101

EXAMINER	
CLARKSON, G.	
ART UNIT	PAPER NUMBER
2501	2

DATE MAILED: 09/25/96

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-25 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-25 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

FCS1688820

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

(g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at

the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The following is a quotation of the appropriate paragrapha of 35 U.S.C. 112 that form the basis for the rejections under this section made in this Office action:

1. The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. The specification shall conclude with one of more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, first and second paragraphs, as the claimed invention is not described in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same, and/or for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant's use of the term "gate" is apparently not known to the semiconductor art. In the art a "gate" is a metal electrode or highly doped region which is biased to produce a depletion region of the semiconductor which is called the "channel." It is unknown in the semiconductor art for an operation where the "gate becomes depleted.". A common gate material is aluminum. How, exactly, does applicant intend for aluminum to "become depleted"? What utility is had for such a "depleted gate"? The specification is unclear. Further, "of the top gate to

device region junction" in claim 2 is a non-sequitur. Since no boundaries are clearly defined, the "peripheral edge" is unclear. The "body contact" of claim 16 has unclear support in the specification. In claim 22, it is not clear if "a semiconductor region" is the same thing as the "a second body" or not. If not, what distinguishes one from the other? Not clear.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by Process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Further, "a drift region" by itself is unclear; all semiconductor regions and materials have thermally generated carries "drift" through them. With "adjacent", it is not clear if "contact" is meant or not.

Claims 1-6, as they can be understood, are rejected under 35 U.S.C. 102(a), (b), (e) and/or (g) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over the Vaes et al. patent. While the claims are not entirely clear, the RESURF structure they appear to be attempting to claim appear to be met by the Vaes et al. patent. Any interpretation of the claims is felt at least obvious over the Vaes et al. patent.

Claims 7, 8, and 11-25, as they can be understood, are rejected under 35 U.S.C. 102 (a), (b), (e) and/or (g) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak. Here Colak shows an upper field-shaping region 30b and a lower field-shaping region 30a. As the claims can be understood, they are met by Colak. Any interpretation of the claims is felt at least obvious over Colak.

Claims 9 and 10, as they can be understood, are rejected under 35 U.S.C. 103 as being unpatentable over Colak as applied to claim 7 above, and further in view of the Vaes et al. patent. The Vaes et al. patent teaches that the same field-shaping considerations needed for a lateral bipolar transistor are the same as that for a lateral MOS desigh. It would be obvious from use Colak's field-shaping means in a lateral bipolar transistor.

Coe shows the equivalency, of the simple drift extension 6 in Figure 1 and having a coextensive drift region, as at Figure 2.

Tihanyi shows another example of the process of ion-implantation used to form various regions in a high voltage field effect transistor.

Sakuma et al. show another example of a high voltage transistor where the drift region is annular to the drain and is surrounded by the source region.

Wagenaar et al. and Singer both show other examples of field-shaping means and are similar to Colak and Vaes et al.

The Vaes et al. article is similar to that of the patent.

All the above references are considered pertinent to the disclosed subject matter.

J. Clawson/wb
(703)-557-4822
9/19/86

Joseph E. Clawson
JOSEPH E. CLAWSON, JR.
EXAMINER
GROUP ART UNIT 253

PTO - 948 (Rev. 6-92)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTACHMENT TO PAPER NUMBER 2

S.N. 831384

GROUP

NOTICE OF PATENT DRAWINGS OBJECTION

Drawing Corrections and/or new drawings may only be submitted in the manner set forth in the attached letter, "Information on How to Effect Drawing Changes" PTO-1474.

A. ☑ The drawings, filed on 2-7-86, are objected to as informal for reason(s) checked below:

1. ☐ Lines Pale.
2. ☐ Paper Poor.
3. ☐ Numerals Poor.
4. ☑ Lines Rough and Blurred.
5. ☐ Shade Lines Required.
6. ☐ Figures Must be Numbered.
7. ☐ Heading Space Required.
8. ☐ Figures Must Not be Connected.
9. ☐ Criss-Cross Hatching Objectionable.
10. ☐ Double-Line Hatching Objectionable.
11. ☐ Parts in Section Must Be Hatched.
12. ☐ Solid Black Objectionable.
13. ☐ Figure Legends Placed Incorrectly.
14. ☐ Mounted Photographs.
15. ☐ Extraneous Matter Objectionable. [37 CFR 1.84 (l)]
16. ☑ Paper Undersized; either 8½" x 14", or 21.0 cm. x 29.7 cm. required.
17. ☐ Proper A4 Margins Required:
    ☐ TOP 2.5 cm. ☐ RIGHT 1.5 cm.
    ☐ LEFT 2.5 cm. ☐ BOTTOM 1.0 cm.
18. ☐ Other:

B. ☑ The drawings, submitted on 2-7-86, are so informal they cannot be corrected. New drawings are required. Submission of the new drawings MUST be made in accordance with the attached letter.

FCS1688826

...OP AND BOTTOM EDGES, SNAP—APART AND DISCARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
831,384	253	2

APPLICANT(S): BEASOM

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4270137	5-81	COE	357	23.4	
	B	4300150	11-81	COLAK	357	13	
	C	4394680	8-83	TIHANYI	357	23.8	
	D	4394674	7-83	SAKUMA ET AL	357	23.8	
	E	4409606	10-83	WAGENAAR ET AL	357	23.8	
	F	4422089	12-83	VAES ET AL	357	23.F	
	G	4485392	11-84	SINNEK	357	23.F	
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R H. VAES ET AL, "HIGH-VOLTAGE, HIGH CURRENT LATERAL DEVICES," 1980 IEDM CONF PROC, DEC. 8-10, 1980, pp. 87-90.

S

T

U

EXAMINER	DATE
JOSEPH CLAWSON	9-18-86

*A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)

FCS1688827

GP 253

#3
4-7-87

HARRIS

Case SE-395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:	
Applicant:	James D. Beason
Serial No.:	831,384
Filed:	January 7, 1986
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	Joseph E. Clawson, Jr.

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

PETITION FOR EXTENTION OF TIME

Pursuant to 37 C.F.R. 1.136, Applicant petitions for extension of time for filing the amendment attached herewith for the above-identified application. The amendment was due within the shortened statutory time perion ending on December 25, 1986. Please charge the fee of $390.00 for the three month extension of time to the deposit account of Harris Corporation, Deposit Account No. 08-0870.

The Commissioner is hereby authorized to charge any additional required fees pr credot any overpayment to the above account. An additional copy of this sheet is attached.

Respectfully Submitted,

Thomas N. Twomey

Thomas N. Twomey
Reg. No. 28,916
(305) 729-4508

S 20583 04/03/87 831384 08-0870 020 117 390.00CH

HARRIS CORPORATION SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FLORIDA 32901

#4

HARRIS

Case SE-395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED

APR 06 1987

GROUP 250

In re Patent Application:	
Applicant:	James D. Beason
Serial No.:	831,384
Filed:	January 7, 1986
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	Joseph E. Clawson, Jr.

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir: LETTER OF TRANSMITTAL

For: ✓ an Amendment for filing and,

✓ a Petition for Extension of Time.

____ A check in the amount of $_____ is enclosed.

__X__ The Commissioner is hereby authorized to charge the above-noted and any additional fees which may be required, or credit any overpayment to Account No. 08-0870. A duplicate copy of this sheet is enclosed.

Thomas N. Twomey

THOMAS N. TWOMEY
Sector Patent Counsel
Reg. No.: 28,916
Phone: (305) 729-4508

Date of Signature

3/18/87

Signature

Registered Representative

Name of applicant, assignee or

THOMAS N. Twomey

(Date of Deposit)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 3/18/87

HARRIS CORPORATION SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FLORIDA 32901

FCS1688829

Attorney Docket SE-395

4/a
SR
4-7-87

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:	
Applicant:	James D. Beasom
Serial No.:	831,384
Filed:	1/7/86
For:	High Voltage Lateral MOS Structure
Group Art Unit:	253
Examiner:	Joseph E. Clawson, Jr.

AMENDMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

The following amendments and remarks are respectfully submitted in response to the Office Action mailed Sept. 25, 1986 in connection with the above-identified application.

Attorney Docket SE-395

IN THE SPECIFICATION:
Please amend the Specification as follows:

Page 11, line 4, following "ion implanted" please insert -- into the drift region --.

Page 11, line 10, following "top gate 21 are diffused" please insert -- into the body 11--.

IN THE CLAIMS:

Please cancel Claims 1, 2, 11, 13, 14, and 21 without prejudice or disclaimer of the subject matter thereof.

Please amend the Claims as follows:

Please rewrite claims 3 and 12 as follows:

3. (amended) In a [A] semiconductor device [as claimed in claim 2] of the type including a lateral drift region of a first conductivity type, said drift region serving as a JFET channel, the improvement comprising:

providfng a top gate of a semiconductor material having a second conductivity type over said drift region to cause depletion of said drift region from both top ~~and bottom~~ upon application of a reverse bias voltage to said device,

wherein said top gate laterally abutts a device region to form a junction and said top gate becomes depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction, and

wherein said top gate becomes depleted at a reverse bias voltage less than [then] the reverse bias voltage at which said drift region becomes depleted.

12. (amended) A lateral MOS structure [as claimed in claim 11 wherein:] comprising a semiconductor body of a first conductivity type, source and drain regions of a second ~~conductivity~~ type forming respective source and drain junctions with said body; and a drift region of said second conductivity type, said drift region forming a JFET channel in said body controlled by said semiconductor body which body operates as a JFET gate such that upon application of a reverse bias to said body to drain junction said drift region becomes depleted, and

a top gate of said first conductivity type formed in said drift region, said top gate [becomes] becoming depleted below a body to drain voltage at which [the] said drift region becomes depleted.

Please amend claims 19 and 21 as follows:

Claim 19, first line, delete "11" and in its place insert --12--.

Claim 21, first line, delete "11" and in its place insert --12--.

Please rewrite claim 22 as follows:

22. (amended) [In] A diode structure comprising:

a first semiconductor body of a first conductivity type contained within [in] a semiconductor region of a second conductivity type and forming a diode junction therewith, said semiconductor region having a first dopant concentration, [and]

a second body of said [second] first conductivity type contained within said semiconductor region and having a second dopant concentration greater

than said first dopant concentration, said second body [completely]surrounding the lateral perimeter of said first body and abutting said first body [adjacent thereto];

Cont'd C3

said second body forming a JFET channel controlled by said semiconductor region which region operates as a JFET gate such that upon application of a reverse bias to said region to first body junction said second body becomes depleted, [the improvement comprising:] and

a top gate of said second conductivity type formed [over] within said second body, said top gate having a dopant concentration such that upon application of said reverse bias, said top gate becomes depleted before said second body becomes depleted.

REMARKS

Claims 1-25 were rejected under 35 U.S.C. sec. 112, first and second paragraphs, based on the following points.

1) The Examiner states that it is unknown in the semiconductor art for an operation where the "gate becomes depleted." Additionally, the Examiner stated, applicant's use of the term "gate" is apparently unknown in the semiconductor art.

It is acknowledged that applicant's use of the term "gate" goes beyond its most common usage, as pointed out by the Examiner. However, applicant submits that the structure described in the application operates to cause depletion of a channel-type region (the drift region), just as does a conventional gate, and as such, reference to this structure as a gate might actually cause less confusion than would be caused by selection of a previously unknown term. It is noted that applicant has uniformly called the new structure a "top gate" which is believed to provide enough information, particularly in view of the descriptions in the specification of applicant's structure, to permit one of ordinary skill in the art to understand that which applicant is describing. Still further, applicant has amended the claims to specify that the top gate is of a semiconductor material since, as pointed out by the Examiner, depletion of a metal gate is not intended.

The Examiner has inquired as to the utility of a depleted top gate. (While it appears that this question may have been directed to the aluminum gate mentioned by the Examiner, and applicant, as stated below

does not intend to claim metal top gates, the following explanation is provided.) The depletion of a top gate is significant in that its depletion assures that a large top gate to drain voltage is not developed by punch-through action from the body. This is mentioned in the specification at the top of page 10. The reason this is desired during extreme reverse bias conditions is that the invention is directed to a structure which can withstand extreme reverse bias yet have a low ON-resistance. By depleting the top gate during extreme reverse bias conditions the breakdown voltage of the drain junction is maximized.

Applicant has also amended the specification at page 11 to expressly indicate that the top gate is formed of the semiconductor material of the starting materials, a fact which can be ascertained by reading the specification but which was not previously expressly stated. This amendment does not add new matter since the process description clearly indicates that the top gate is formed in the substrate by impurity introduction, a step which obviously could only be accomplished if the top gate is being formed in the substrate.

2) The Examiner has identified a non-sequitur in claim 2. Notwithstanding that claim 2 has been cancelled, this defect has been corrected by providing an antecedent basis for the recited junction and

peripheral edge in the claim language which now appears in the rewritten claim 3.

3) The Examiner has indicated that the "body contact" called for in claim 16 does not have clear support in the specification. The Examiner's attention is directed to the Specification at page 12, near the bottom of the page where Applicant has described what is meant by a body contact. It is respectfully submitted that the body contact called for in claim 16 is similar in type to the body contact 11c described commencing at the bottom of page 12 of the specification. This description expressly states that the body contact and top gate overlap and that the dopant concentration in the body contact is higher than that in the the drift region (the concentration in the body contact overcomes the dopant in region 17) and clearly communicates to one of ordinary skill in the semiconductor art that the conductivity type of the body contact is of the "first conductivity type" called for in the claim. It would be well understood that a "body contact" is of the same conductivity type as the body. Applicant submits that the disclosure is sufficient to enable one of ordinary skill in the art to understand the body contact as called for in the claims.

4) The Examiner has questioned the clarity of claim 22 regarding the description of the "semiconductor region" and the "second body" and

their relationship. This claim has been amended to clarify that the recited claim elements are generally like those shown in figure 9, where the first body is like the drain 12, the semiconductor region is like the substrate 11, the second body is like the region 17 and the top gate is like the top gate 21. The claim as rewritten defines the structure in a manner which can be more readily understood.

5) The Examiner has indicated that "drift region" and "adjacent" are unclear. The claims have been amended to more completely define the characteristics which result in a drift region. With respect to the term adjacent, the Examiner is correct that adjacent may mean either that there is or is not necessarily contact. The first definition of "adjacent" in Webster's Ninth New Collegiate Dictionary, Merriam-Webster Inc., Springfield, Massachusetts, 1984 reads: "not distant : NEARBY... [the definition goes on to explain]...ADJACENT may or may not imply contact but always implies absence of anything of the same kind in between..." It is applicant's intention that the claim shall cover structures where there is contact as well as those where the two regions are near one another, where such a structure is otherwise capable of meeting the claim limitations. It is submitted that, for instance, top gate operation may be achieved even if a thin dielectric is interposed between the drift region and the top gate of the structure of claim 7. While this option was not contemplated at

the time of filing, it does not appear necessary to expressly disclaim this obvious variation of the disclosed embodiments of the invention.

Claims 1-6 were rejected under 35 U.S.C. sec. 102(a), (b), (e) and/or (g) or in the alternative under 35 U.S.C. sec. 103 over the Vaes patent. The Examiner stated that "the RESURF structure [the claims] appear to be attempting to claim appear to be met by the Vaes et al. patent."

It is submitted that the claims, as amended, patentably distinguish over Vaes et al. All claims presented in the application specify that the top gate becomes depleted before the underlying drift region. Vaes does not disclose or suggest this relationship. It is desirable to insure that the top gate depletes prior to the depletion of the adjoining drift region in order that depletion of the top gate may be reliably achieved. If the drift region were to become depleted prior to the depletion of the top gate, there would be no remaining charge in the drift region for field line termination except through the ends of the top gate, such as into the abutting device region.

Another distinction between my device and that of Vaes arises from the fact that he uses the substrate to device region PN junction beneath the device (the bottom part of the isolation junction as a necessary part of his invention. In all cases, the substrate (P) to adjacent overlying

device island region (N) PN junction acts to deplete a part of that N island region (which must be totally depleted for proper operation of his devices).

The present invention works without limitation on the isolation. It may be used with no isolation as for a discrete device or a self-isolated MOS process. It can also be used with isolation methods which do not use PN junctions for isolation such as dielectric isolation.

One significant limitation which arises from using the isolation junction as an active part of the breakdown voltage improvement structure is punch through from the substrate (P) to device region (P) in the isolated island (N) when there is a large device region to substrate voltage. Vaes recognises the problem in col. 2 l. 6-13 and col. 2 l. 30-31 where he states that one of his objectives is to reduce the problem. In the devices of the present invention, the problem is completely eliminated resulting in a significant improvement in flexability of circuit application of devices made in accordance with it compared to those made according to Vaes. The present invention provides a reliable solution to the problem of punch through at high voltages which solution is not mentioned in the known prior art. Reconsideration of the rejection(s) over Vaes et al is respectfully requested.

Claims 7,8, and 11- 25 were rejected under 35 U.S.C. sec. 102(a), (b), (e) and/or (g) or in the alternative under 35 U.S.C. sec. 103 over Colak. The Examiner stated that Colak shows an upper field shaping region 30b and lower field shaping region 30a.

Applicant respectfully submits that the claims are neither anticipated nor rendered obvious by Colak. Nothing in Colak shows first and second device regions of a second conductivity type in a body of a first conductivity type. In Colak, layer 12 appears to be an epitaxial layer in which the device regions are formed. This epitaxial region, as shown in figure 4 is of the same conductivity type as the device regions 14 and 20. Further, the claims call for the drift region to be formed in the body while Colak forms the epitaxial layer on the body. If Colak is deemed to show that the epi layer is the body, then the device regions are not formed in a body of the opposite conductivity type while if the epi layer is not deemed to be the body, then the device regions are not formed in the body. Thus, Colak does not anticipate the claims. Further, the differences in structure between Colak and the claimed structure render it difficult to understand how an obviousness assertion can be made in view of the amended claims. It is not seen how Colak discloses or suggests that any top gate becomes depleted at a lower reverse bias voltage than the drift region, a feature now called for in each of the claims presently presented in the application.

Claims 9 and 10 were rejected under 35 U.S.C. sec. 103 over Colak in view of Vaes. For the reasons explained hereinabove, it is submitted that these references do not suggest that the top gate will become depleted at a lower reverse bias voltage than is required to totally deplete the drift region.

The independent claims presented for reconsideration 3, 7, 12, and 22 each call for depletion of the top gate at a reverse bias voltage below the reverse bias voltage required to totally deplete the drift region. Applicant has pointed out that the references do not disclose this feature of the invention and does not find any suggestion of this feature of the invention in the references.

The remaining claims are dependent on the independent claims addressed hereinabove and are believed to be allowable therewith. Reconsideration and allowance of the present application are respectfully requested in view of the amended claims, and the explanations provided herein regarding the differences between the prior art and the invention.

Attorney Docket SE-395

Please charge any additional fees or credit any overpayments to the deposit account of Harris Corporation, Account Number 08-0870. An additional copy of this sheet is attached.

Respectfully submitted,

Thomas N. Twomey

Reg. No. 28,916

(305) 729-4508

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
06/831,384	01/07/86	BEASOM	SE-375

THOMAS N. TWOMEY
SECTOR PATENT COUNSEL
HARRIS SEMICONDUCTOR
P. O. BOX 883
MELBOURNE, FL 32901-0101

EXAMINER	
CLARSON JR J	
ART UNIT	PAPER NUMBER
253	5

DATE MAILED: 07/10/87

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 3-23-87 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 3-10, 12, 15-20, 22-25 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☒ Claims 1, 2, 11, 13, 14, 21 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 3-10, 12, 15-20, 22-25 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

FCS1688844

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless-
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
>
> (g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the

subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 112 that form the basis for the rejections under this section made in this Office action:

2. The specification shall conclude with one of more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-6, as now amended, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims have now been amended to read that the "top gate" causes depletion of the drift region not only on the top but "both top and bottom ". There are no recited structures or means which would clearly produce this desired effect. The claims are thus unclear at this point. Applicant's clarification of the other terms and their meaning, and the amendments to the claims therein, have been helpful and greatly appreciated by the Examiner.

Claims 3-6, 12 and 15-20 as now amended, and claims 7-10 are rejected under 35 U.S.C. 103 as being unpatentable over Colak and Singer of record considered together. Colak shows a lateral transistor with a drift region and also shows a reduced surface field region 30b of opposite conductivity contacting the main region 20 and additionally drawing a buried field control region 30a. It is well known that a lightly doped semiconduc-

tor region can be "depleted" of its free carriers more easily than a more highly doped semiconductor region. While Colak does not expressly provide absolute or relative doping values for all of his regions, Singer shows that such surface field reducing regions such as his region 20 may be more lightly doped than the drift region in which they reside ($4x10^{14}$ vs. $5x10^{14}$). It would be obvious to one of ordinary skill in the art to use Singer's doping levels in Colak's device since they are both concerned with the same RESURF problems.

Claims 22-25, as now amended, are rejected under 35 U.S.C. 103 as being unpatentable over Colak and Singer as applied to claim 3 above, and further in view of the Vaes et al literature article, of record. Vaes et al show, e.g. at Figures 7 and 9 that both upper and lower RESURF regions ("gate") are adjacent the drift region and more lightly doped than the drift region. Also, a circularly symmetric device would be obvious to one of ordinary skill in the art. It would be obvious to use such teachings of the Vaes et al article in Colak and Singer, all of record.

Since claims 7-10 have been given a new ground of rejection based upon Applicant's explanation of his invention, a further discussion of applicant's Remarks will be held in abeyance until he has had an opportunity to respond to this action.

Any inquiry concerning this communication should be directed to J. Clawson at telephone number 703-557-4822.

J. Clawson/gd

6-23-87

Joseph E. Clawson

JOSEPH E. CLAWSON
EXAMINER
GROUP ART UNIT 253

4253

HARRIS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#6
SL
12-16-87

e Patent Application:

Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

HONORABLE COMMISSIONER OF
PATENTS AND TRADEMARKS
WASHINGTON, D.C. 20231

PETITION FOR EXTENSION OF TIME

Pursuant to 37 CFR §1.136, applicant petitions for extension of time for filing the amendment attached herewith for the above-identified application. The amendment was due within the shortened statutory time period ending on October 30, 1987. Please charge the fee of $170.00 for the 2 month extension to the deposit account of Harris Corporation 08-0870.

The Commissioner is hereby authorized to charge any additional required fees or credit any overpayment to the above account. An additional copy of this sheet is attached.

Respectfully submitted,

William A. Troner
Reg. No. 32,316

Phone (305) 729-4508

016/D

S 20608 12/10/87 831384 08-0870 020 116 170-020X

HARRIS

Attorney Docket SE-395

COMMISSIONER OF PATENTS AND TRADEMARKS

In re Patent Application:

Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

CERTIFICATE OF MAILING 37 C.F.R. 1.8(a)

I hereby certify that the attached Petition for Extension of Time is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

on the date indicated below.

DATE: December 1, 1987 BY:

Diana Desjardins
Secretary to
William A. Troner
Reg. No 32,316
(305) 729-4511

HARRIS CORPORATION SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FLORIDA 32901

HARRIS

#7

Attorney Docket SE-395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:	
Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

AMENDMENT TRANSMITTAL LETTER

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment to an Office Action for filing and the filing fee is calculated below:

	No. After Amendment		Highest No. Prev. Filed		No. Extra	Rate	Fee
Total claims	19	-	* 20=	0		X $12	$ 0
Independent claims	04	-	* 04=	0		X $34	$ 0
						TOTAL:	$ 0

* If less than 20, enter 20
** If less than 3, enter 3

____ A check in the amount of $_____ is enclosed.

_X_ The Commissioner is hereby authorized to charge the above-noted and any additional fees which may be required, or credit any overpayment to Account No. 08-0870. A duplicate copy of this sheet is enclosed.

WILLIAM A. [illegible]

Reg. No.: 32,[illegible]

Phone: (305) 729-4511

WAT/DD

HARRIS CORPORATION SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FLORIDA 32901

Patent Attorney

Attorney Docket SE-395

7/13
10L
12/16/87

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:

Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

AMENDMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

The following amendments and remarks are respectfully submitted in response to the Office Action mailed 7/10/87 in connection with the above-identified application.

Attorney Docket SE-395

IN THE CLAIMS:

Please amend the following claims as follows:

Claim 3, line 1, after "A" insert --dielectrically isolated--;

line 6, after "both" insert --the--;

after "top" delete "and bottom".

Claim 7 (Once Amended)

A semiconductor device comprising:

a semiconductor body of a first conductivity type;

a first device region of a second conductivity type formed in said body;

a second device region of said second conductivity type formed in said body and separated from said first device region;

a drift region of said second conductivity type formed in said body between said first and second device regions, separated from said second device region by a separation zone and in contact with said first device region, said drift region having a first side adjacent said body;

a top gate of said first conductivity type adjacent a substantial portion of a second side of said drift region;

wherein said top gate and semiconductor body operate as a top and bottom gate respectively of a JFET channel formed by said drift region;

said top gate becoming depleted at a body to first device region voltage below the voltage at which the body to drift region depletion layer in said first side of said drift region reaches the top gate to drift region depletion layer in said second side of said drift region.

Claim 12, line 3, change "conducitvity" to --conductivity--.

Claim 15, line 1, change "11" to --12--.

Claim 16, line 1, change "11" to --12--.

Claim 17, line 1, change "11" to --12--.

Claim 18, line 1, change "11" to --12--.

REMARKS:

Claims 3-6 were rejected under 35 USC §112, second paragraph. Independent Claim 3 has been amended to obviate the rejection. Specifically, claim 3 has been amended to clarify that the top gate causes depletion of the drift region from the top upon application of a reverse bias voltage.

Claims 3-10, 12, 15-20 were rejected under 35 USC §103 as being unpatentable over Colak and Singer. Claims 22-25 were rejected under 35 USC §103 over Colack, Singer and the Vaes et al article. These rejections are respectfully traversed.

The present invention relates to high voltage lateral devices having reduced ON resistance. In a preferred embodiment, this reduced ON resistance is translated into reduction in channel resistance, which is accomplished by the addition of a top gate located between a lateral drift region and the surface of the channel region. Both the top gate and drift region are formed in the semiconductor body.

The art of record discloses various RESURF mechanisms formed in a device where the layer designed for depletion, e.g. the buried layer, also functions as part of the isolation mechanism for the device itself. As a result, the substrates in these devices must assume the most negative voltage in the devices to provide the isolation junction. This bias reduces the ability to reduce the punch through from the device regions to the substrate because it does not permit the body of the device to work in conjunction with the top gate as a JFET such that the JFET channel, e.g. the drift region, can be effectively biased. The present invention, as now claimed, does not require the substrate or body to be biased as such because the substrate or body does not participate as part of the isolation mechanism. As a result, the present invention can more effectively provide high voltage protection without increasing resistance of the channel path.

In veiw of the interview discussion and the foregoing amendments and remarks, favorable consideration upon all the claims in the application is respectfully requested. In the event that there are any questions concerning this Amendment or the Application in general, a telephone call to the undersigned would be greatly appreciated.

Attorney Docket SE-395

Please charge any additional fees or credit any overpayments to the deposit account of Harris Corporation, Account Number 08-0870. An additional copy of this sheet is attached.

Respectfully submitted,

William A. Troner

William A. Troner

Registration No. 32,316

(305) 729-4511

WAT/DD

Attorney Docket SE-395

Please charge any additional fees or credit any overpayments to the deposit account of Harris Corporation, Account Number 08-0870. An additional copy of this sheet is attached.

Respectfully submitted,

William A. Troner

William A. Troner

Registration No. 32,316

(305) 729-4511

WAT/DD

HARRIS

MAIL ROOM 17 DEC 3 1987 PAT. & TRADEMARK OFF.

Attorney Docket SE-395

COMMISSIONER OF PATENTS AND TRADEMARKS

In re Patent Application:

Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

RECEIVED Dec 14 9 05 AM '87 U.S. PATENT AND TRADEMARK OFFICE

CERTIFICATE OF MAILING 37 C.F.R. 1.8(a)

I hereby certify that the attached Amendment to an Office Action is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

on the date indicated below.

DATE: December 1, 1987 BY:

Diana Desjardins

Diana Desjardins
Secretary to
William A. Troner
Reg. No. 32,316
(305) 729-4511

HARRIS CORPORATION . SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FLORIDA 32901

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
06/831,384	01/07/86	BEASOM J	SE-395

THOMAS N. THOMEY
SECTOR PATENT COUNSEL
HARRIS SEMICONDUCTOR
P. O. BOX 883
MELBOURNE, FL 32901-0121

EXAMINER	
CLAWSON JR, J	
ART UNIT	PAPER NUMBER
253	5

DATE MAILED: 03/08/89

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 12-3-87 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ___ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:
1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 3-10, 12, 15-20, 22-25 are pending in the application.
Of the above, claims _____ are withdrawn from consideration.
2. ☒ Claims 1, 2, 11, 13, 14, 21 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 3-10, 12, 15-20, 22-25 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

FCS1688861

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless-
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
>
> (g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (E) and (g) of section 102 of this title, shall not

preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 112 that form the basis for the rejections under this section made in this Office action:

1. The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. The specification shall conclude with one of more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-6, as now amended, are rejected under 35 USC 112, paragraph 1, as lacking sufficient supporting disclosure to enable anyone skilled in the art to be able to make and use the same, and appear to be directed toward new matter. The claims have all now been amended to read "a dielectrically isolated semiconductor device", but there is apparently a lack of supporting disclosure to enable anyone skilled in the art to be able to make and use the same, and such is apparently new matter.

Claims 3-10, 12 and 15-20 as now amended, and as they can be understood in light of the enabling disclosure, are rejected under 35 U.S.C. 103 as being unpatentable over Colak and Singer of record considered together. Colak shows a lateral transistor with a drift region and also shows a reduced surface field region 30b

of opposite conductivity contacting the main region 20 and additionally drawing a buried field control region 30a. It is well known that a lightly doped semiconductor region can be "depleted" of its free carriers more easily than a more highly doped semiconductor region. While Colak does not expresaly provided absolute or relative doping values for all of his regions, Singer shows that such surface field reducing regions such as his region 20 may be more lightly doped than the drift region in which they reside ($4x10^{14}$ vs. $5x10^{14}$). It would be obvious to one of ordinary skill in the art to use Singer's doping levels in Colak's device according to his teachings since they are both concerned with the same RESURF problems.

Claims 22-25 stand rejected under 35 U.S.C. 103 as being unpatentable over Colak and Singer as applied to claim 3 above, and further in view of the Vaes et al literature article, of record. Vaes et al show, e.g. at Figures 7 and 9 that both upper and lower RESURF regions ("gate") are adjacent the drift region and more lightly doped than the drift region. Also, a circularly symmetric device is a common design and would be obvious to use to one of ordinary skill in the art. It would be obvious to use such teachiags of the Vaes et al article in Colak and Singer, all of record, due to the greater device control.

It is argued, page 4 of the Remarks of Paper No. 7, that the invention derives from "the addition of a top

gate...". However, top gates such as described are well-known in the semiconductor art. The further assertion that "Both the top gate and the drift region are formed in the semiconductor body", but both Singer and Vaes et al show this conventional construction.

It is further argued that in the invention "the substrate or body does not participate as part of the isolation mechanism...". However, the does not appear to be any workable "isolation mechanism" disclosed.

Applicant's arguments filed December 3, 1987, have been fully considered but they are not deemed to be persuasive.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

This action is a final rejection and is intended to close the prosecution of this application. Applicant's response to this action is limited either to an appeal to the Board of Appeals or to an amendment complying with the requirements set forth below.

If applicant should desire to appeal any rejection made by the examiner, a Notice of Appeal must be filed within the period for response identifying the rejected claim or claims appealed. The Notice of Appeal must be accompanied by the required appeal fee of appropriate amount.

If applicant should desire to file an amendment, entry of a proposed amendment after final rejection cannot be made as a matter of right unless it merely cancels claims or complies with a formal requirement made earlier. Amendments touching the merits of the application which otherwise might not be proper may be admitted upon a showing of good and sufficient reasons why they are necessary and why they were not presented earlier.

The filing of an amendment after final rejection, whether or not it is entered, does not stop the running of the statutory period for response to the final rejection unless the examiner holds the claims to be in condition for allowance. Accordingly, if a Notice of Appeal has not been filed properly within the period for response or any extension of the period obtained under either 37 CFR 1.136(a) or (b), the application will become abandoned.

JOSEPH E. CLAWSON JR.
EXAMINER
GROUP ART UNIT 253

J. Clawson/gd

(703)557-4822

2-29-88

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
831384			

EXAMINER	
ART UNIT	PAPER NUMBER
	9

DATE MAILED: 10-4-88

EXAMINER INTERVIEW SUMMARY RECORD

All participants (applicant, attorney, agent) representing applicant:

(1) W. TRONER (3) _____

(2) J. BEASON (4) _____

Date of interview 8-2-88

Type: ☒ Telephonic ☐ Personal (copy is given to applicant).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.

Agreement ☒ was reached with respect to some or all of the claims in question. ☐ was not reached.

Claims discussed: 3

Identification of prior art discussed: SINGER, COLAK

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

THE EXR. SUGGESTED SEVERAL WAYS OF INCORPORATING WHAT APPLICANT CONSIDERS TO BE HIS INVENTION IN THE CLAIMS, SPECIFICALLY THE GUMMEL NUMBER OF HIS REGION 21 AND ITS CONNECTION TO THE BODY 11.

(A fuller necessary description and any available copy of amendments that the examiner agreed would render the claims allowable, or where no copy of the amendments is available, a summary thereof, is attached.)

Joseph F. Clawson Jr.
JOSEPH F. CLAWSON, JR.
EXAMINER
GROUP ART UNIT 253

☒ It is not necessary for applicant to supplement the information on this form or to submit a separate record of the substance of the interview.

APPLICANTS, ATTORNEYS AND AGENTS ARE REMINDED OF THEIR RESPONSIBILITY TO SUPPLEMENT THIS RECORD WITH AN INDICATION OF THE SUBSTANCE OF THE INTERVIEW AS REQUIRED BY 37 CFR 1.133(b) AND SECTION 713.04 OF THE MANUAL OF PATENT EXAMINING PROCEDURE. (See reverse side for text of Section 713.04.)

PTOL-413 (rev. 9/78)

ORIGINAL FOR INSERTION IN RIGHT HAND FLAP OF FILE WRAPPER

MP. 253

Attorney Docket SE-395

CORRES. AND MAIL

BOX AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#10
Reg Ext
FJ
9-14-88

In re Patent Application: Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

Commissioner of Patents and Trademarks
Washington, D. C. 20231

PETITION FOR EXTENSION OF TIME

Pursuant to 37 CFR §1.136, applicant petitions for extension of time for filing the amendment attached herewith for the above-identified application. The amendment was due within the shortened statutory time period ending on June 8, 1988. Please charge the fee of $390.00 for the 3 month extension to the deposit account of Harris Corporation 08-0870.

The Commissioner is hereby authorized to charge any additional required fees or credit any overpayment to the above account. An additional copy of this sheet is attached.

Respectfully submitted,

William A. Troner

William A. Troner
Registration No. 32,316
(407) 729-4511

034/D

N 10427 09/13/88 831384 08-0870 010 117 390.00CH

HARRIS

Attorney Docket SE-395CIPX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:
Applicant(s): JAMES D. BEASOM
Serial No.: 831384
Filed: 1-7-89
For: A HIGH-VOLTAGE LATERAL SEMICONDUCTOR DEVICE

Group Art Unit:
Examiner:

Commissioner of Patents and Trademarks
Washington, D. C. 20231

PETITION FOR EXTENSION OF TIME

Sir:

Pursuant to 37 CFR §1.136, applicant petitions for extension of time for filing the continuation in part attached herewith for the above-identified application. The continuation in part was due within the shortened statutory time period ending on June 8, 1988. Please charge the fee of $390.00 for the 3 month extension to the deposit account of Harris Corporation 08-0870.

The Commissioner is hereby authorized to charge any additional required fees or credit any overpayment to the above account. An additional copy of this sheet is attached.

N 10242 09/13/88 831384 08-0870 010 117 390.00CH

Respectfully submitted,

William A. Troner

William A. Troner
Registration No. 32,316
(407) 729-4511

034/D

HARRIS

Attorney Docket SE-395CIPX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR: JAMES D. BEASOM

INVENTION: A HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

CERTIFICATE OF MAILING BY EXPRESS MAIL

Sir:

This will certify that the enclosed patent application for the above identified invention is being mailed via EXPRESS MAIL on the date indicated below to the Commissioner of Patents and Trademarks, Washington, DC 20231, in an envelope having an Express Mail Label Number: 23069666.

Date Mailed: September 8, 1988

By: William A. Troner

William A. Troner

Registration No. 32,316

(407) 729-4511

033/D HARRIS CORPORATION SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FLORIDA 32901

HARRIS

Attorney Docket SE-395

CORRES. AND MAIL
BOX AF
COMMISSIONER OF PATENTS AND TRADEMARKS

In re Patent Application

Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

CERTIFICATE OF MAILING 37 C.F.R. 1.8(a)

I hereby certify that the attached Petition for Extension of Time is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

on the date indicated below.

DATE: September 8, 1988

BY: William A Troner

William A. Troner
Registration No. 32,316
(407) 729-4511

033/D

HARRIS

CORRES. AND MAIL

BOX AF

Attorney Docket SE-395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:	
Applicant:	JAMES D. BEASON
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

Commissioner of Patents and Trademarks
Washington, D.C. 20231

AMENDMENT TRANSMITTAL LETTER

Sir:

Transmitted herewith is an Amendment to a Final Office Action for filing and the filing fee is calculated below:

	No. After Amendment	Highest No. Prev. Filed	No. Extra	Rate	Fee
Total claims	19	* 20= 0		X $12	$ -0-
Independent claims	04	* 04= 0		X $34	$ -0-
				TOTAL:	$ -0-

* If less than 20, enter 20
** If less than 3, enter 3

____ A check in the amount of $_____ is enclosed.

__X__ The Commissioner is hereby authorized to charge the above-noted and any additional fees which may be required, or credit any overpayment to Account No. 08-0870. A duplicate copy of this sheet is enclosed.

William A. Troner

WILLIAM A. TRONER
Patent Counsel
Registration No. 32,316
(407) 729-4511

032/0

HARRIS

CORRES. AND MAIL

Attorney Docket SE-395

BOX AF

COMMISSIONER OF PATENTS AND TRADEMARKS

In re Patent Application
Applicant: JAMES D. BEASOM
Serial No.: 831,384
Filed: 1/07/86
For: HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit: 253
Examiner: J. E. Clawson, Jr.

CERTIFICATE OF MAILING 37 C.F.R. 1.8(a)

I hereby certify that the attached Amendment to a Final Office Action is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

on the date indicated below.

DATE: September 9, 1988

BY: William A Troner

William A. Troner
Registration No. 32,316
(407) 729-4511

033/0

9-8-88

MAIL ROOM SEP 9 1988 PAT. & TRADE MARK OFF. 32

Attorney Docket SE-395

CORRES. AND MAIL

BOX AF

11/C(W)
FJ
9-14-88
9/19/88

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:	
Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

Commissioner of Patents and Trademarks
Washington, D. C. 20231

OK for Entry

PROPOSED AMENDMENT UNDER 37 C.F.R. §1.116

Sir:

The following proposed amendments and remarks are respectfully submitted in response to the Final Office Action mailed March 8, 1988, in connection with the above-identified application.

Attorney Docket SE-395

IN THE CLAIMS:

Please amend the following Claims as follows:

3. (Thrice Amended) In a [dielectrically isolated] semiconductor device of the type including a lateral drift region of a first conductivity type formed in a body region, said drift region serving as a JFET channel, the improvement comprising:

[providing] a top gate of a semiconductor material electrically connected to said body region and having a second conductivity type over said drift region to cause depletion of said drift region from the top upon application of a reverse bias voltage to said device,

wherein said top gate laterally abutts a device region to form a junction and has a surface area doping density such that said top gate becomes totally depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction, and

wherein said top gate has a surface area doping density such that it becomes totally depleted at a reverse bias voltage less than the reverse bias voltage at which said drift region becomes depleted.

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5. (Twice Amended) A semiconductor device comprising:

a semiconductor body of a first conductivity type;

a first device region of a second conductivity type formed in said body;

a second device region of said second conductivity type formed in said body and separated from said first device region;

a drift region of said second conductivity type formed in said body between said first and second device regions, separated from said second device region by a separation zone and in contact with said first device region, said drift region having a first side adjacent said body;

a top gate of said first conductivity type adjacent a substantial portion of a second side of said drift region and electrically connected to said body;

wherein said top gate and semiconductor body operate as a top and bottom gate respectively of a JFET channel formed by said drift region;

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said top gate having a surface area doping density such that it becomes [becoming] totally depleted at a body to first device region voltage below the voltage at which the body to drift region depletion layer in said first side of said drift region reaches the top gate to drift region depletion layer in said second side of said drift region.

12. (Twice Amended) A lateral MOS structure comprising a semiconductor body of a first conductivity type, source and drain regions of a second conductivity type forming respective source and drain junctions with said body, and a drift region of said second conductivity type, said drift region forming a JFET channel in said body controlled by said semiconductor body which body operates as a JFET gate such that upon application of a reverse bias to said body to drain junction said drift region becomes depleted, and

a top gate of said first conductivity type formed in said drift region and being electrically connected to said body, said top gate having a surface area doping density such that it becomes [becoming] totally depleted below a body to drain voltage at which said drift region becomes depleted.

22. (Twice Amended) A diode structure comprising:

a first semiconductor body of a first conductivity type contained within a semiconductor region of a second conductivity type and forming a diode junction therewith, said semiconductor region having a first dopant concentration,

a second body of said first conductivity type contained within said semiconductor region and having a second dopant concentration greater than said first dopant concentration, said second body surrounding the lateral perimeter of said first body and abutting said first body;

said second body forming a JFET channel controlled by said semiconductor region which region operates as a JFET gate such that upon application of a reverse bias to said region to first body junction said second body becomes depleted, and

a top gate of said second conductivity type formed within said second body and being electrically connected to said first semiconductor region, said top gate having a dopant concentration such that upon application of said reverse bias, said top gate becomes totally depleted before said second body becomes depleted.

REMARKS:

The Examiner in charge, Mr. Clawson, is thanked for the time and courtesies extended to the Applicant and Applicant's Counsel during the telephone interview of August 2, 1988. The substance of the interview, as detailed below, was very helpful in the preparation of this response.

Claims 3-10, 12, and 15-20 were rejected under 35 USC §103 as being unpatentable over Colak and Singer. These rejections are respectfully traversed in view of the above proposed amendments and the remarks below.

The present invention relates to a high voltage lateral device having a reduced ON resistance. In a preferred embodiment, this reduced ON resistance is translated into reduction in channel resistance, which is accomplished by the addition of a top gate located between a lateral drift region and the surface of the channel region. Both the top gate and drift region are formed in a semiconductor body region, with the drift region serving as a JFET channel and the top gate and body region operating as a top and bottom gate respectively of the JFET channel drift region.

The invention as now claimed teaches that the top gate has a surface area doping density such that it becomes totally depleted at a reverse bias voltage below the reverse breakdown voltage of the top gate to device region junction, as well as becoming totally depleted at a reverse bias voltage

less than the reverse bias voltage at which the drift region becomes depleted (see the last paragraph on page 9). In order to accomplish the above, the claimed invention further provides that the top gate is tied to the body region such that, upon reverse bias of the major PN junction between the device region and the body, the top gate is also reversed biased with respect to the device region.

Applicant respectfully submits that the invention as now claimed in amended claims 3, 7, 12 and 22 is not rendered obvious in by Colak or Singer. Neither Colak nor Singer teaches having an electrical connection between the semiconductor body and the top layer of their devices. Rather, because of the nonspecificity in these references as to the connection of the top layer, it is unknown whether or not these layers could be actually at a floating potential. Thus, Colak and Singer neither show nor suggest the structural features of the invention. Additionally, neither reference indicates that the surface area doping density should be such as to require total depletion of the respective top layers under the conditions claimed in the present invention. Thus, neither Colak nor Singer shows nor suggests the invention as presently claimed in claims 3-10, 12, and 15-20.

Claims 22-25 were rejected under 35 USC §103 as being unpatentable over Colak and Singer in view of Vaes et al. In addition to the reasons explained above, it is submitted that these three references do not suggest

that the top gate will become totally depleted at a lower reverse bias voltage than is required to totally deplete the drift region. Therefore, reconsideration of the rejections over these references is respectfully requested.

The Section 112 rejection has been noted and claim 3 amended to obviate this rejection. In view of the interview discussion and the foregoing amendments and remarks, favorable consideration upon the claims remaining in the application is respectfully requested. In the event that there are any questions concerning this Amendment or the Application in general, a telephone call to the undersigned would be appreciated.

Please charge any additional fees or credit any overpayments to the deposit account of Harris Corporation, Account Number 08-0870. An additional copy of this sheet is attached.

Respectfully submitted,

William A. Troner

William A. Troner
Registration No. 32,316
(407) 729-4511

WAT/DD

that the top gate will become totally depleted at a lower reverse bias voltage than is required to totally deplete the drift region. Therefore, reconsideration of the rejections over these references is respectfully requested.

The Section 112 rejection has been noted and claim 3 amended to obviate this rejection. In view of the interview discussion and the foregoing amendments and remarks, favorable consideration upon the claims remaining in the application is respectfully requested. In the event that there are any questions concerning this Amendment or the Application in general, a telephone call to the undersigned would be appreciated.

Please charge any additional fees or credit any overpayments to the deposit account of Harris Corporation, Account Number 08-0870. An additional copy of this sheet is attached.

Respectfully submitted,

William A. Trotter

William A. Trotter
Registration No. 32,316
(407) 729-4511

WAT/DD

MP. 253

HARRIS

CORRES. AND MAIL

BOX AF

Attorney Docket SE-395

#12 Notice of Appeal FJ 9-14-88

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:	
Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

Commissioner of Patents and Trademarks
Washington, D. C. 20231

NOTICE OF APPEAL

Sir:

Applicant hereby appeals to the Board of Appeals from the decision mailed March 14, 1988, of the Primary Examiner rejecting Claims 1-16.

Please charge the Deposit Account of Harris Corporation, Account Number 08-0870, in the amount of $130.00. A duplicate copy of this sheet is attached.

It is respectfully requested that, if necessary to effect a timely response, this paper be considered as a Petition for an Extension of Time sufficient to effect a timely response and shortages in other fees, be charged, or any overpayment in fees be credited to the Account of Harris Corporation, Deposit Account No. 08-0870.

Respectfully submitted,

William A. Troner

William A. Troner
Registration No. 32,316
(407) 729-4508

043/D

N 10428 09/13/88 831384 08-0870 010 119 130.00CH

HARRIS

CORRES. AND MAIL

BOX AF

Attorney Docket SE-395

COMMISSIONER OF PATENTS AND TRADEMARKS

In re Patent Application	
Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

CERTIFICATE OF MAILING 37 C.F.R. 1.8(a)

I hereby certify that the attached Notice of Appeal is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

on the date indicated below.

DATE: September 8, 1988

BY: William A. Troner

William A. Troner
Registration No. 32,316
(407) 729-4511

033/D

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/881,384	01/07/86	BEASOM J	SE-395

THOMAS N. TWOMEY
SECTOR PATENT COUNSEL
HARRIS SEMICONDUCTOR
P. O. BOX 883
MELBOURNE, FL 32901-0101

EXAMINER	
CLAWSON JR, J	
ART UNIT	PAPER NUMBER
253	13

DATE MAILED: 10/04/88

NOTICE OF ALLOWABILITY

PART I.

1. ☒ This communication is responsive to AMEND 9-9-88
2. ☒ All the claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
3. ☒ The allowed claims are 3-10, 12, 15-20, 22-25.
4. ☐ The drawings filed on _____ are acceptable.
5. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has [...] been received. [...] not been received. [...] been filed in parent application Serial No. _____, filed on _____
6. ☐ Note the attached Examiner's Amendment.
7. ☐ Note the attached Examiner Interview Summary Record, PTOL-413.
8. ☐ Note the attached Examiner's Statement of Reasons for Allowance.
9. ☐ Note the attached NOTICE OF REFERENCES CITED, PTO-892.
10. ☐ Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449.

PART II.

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

1. ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
2. ☒ APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
   a. ☐ Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No. _____. CORRECTION IS REQUIRED.
   b. ☐ The proposed drawing correction filed on _____ has been approved by the examiner. CORRECTION IS REQUIRED.
   c. ☐ Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
   d. ☒ Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:
- _ Examiner's Amendment
- _ Examiner Interview Summary Record, PTOL-413
- _ Reasons for Allowance
- _ Notice of References Cited, PTO-892
- _ Information Disclosure Citation, PTO-1449
- _ Notice of Informal Application, PTO-152
- 1 Notice re Patent Drawings, PTO-948
- _ Listing of Bonded Draftsmen
- _ Other

JOSEPH E. CLAWSON JR.
EXAMINER
GROUP ART UNIT 253

PTOL-37 (REV. 2-85)

USCOMM-DC 6583-P44

FCS1688886

PTOL-85 (REV 4-86)

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

THOMAS H. THOMEY
SECTOR PATENT COUNSEL
HARRIS SEMICONDUCTOR
P. O. BOX 883
MELBOURNE, FL 32901-0101

All communications regarding this application should give the serial number, date of filing, name of applicant, and batch number.

Please direct all communications to the Attention of "OFFICE OF PUBLICATIONS" unless advised to the contrary.

The application identified below has been examined and found allowable for issuance of Letters Patent. PROSECUTION ON THE MERITS IS CLOSED.

SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
06/831,384	01/07/86	019	CLAWSON JR, J	258	10/04/88

First Named Applicant: BEASOM, JAMES D.

TITLE OF INVENTION: HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION (AS AMENDED)

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
SE-395	357-022.000	882	UTILITY	NO	$560.00	01/04/89

The amount of the issue fee is specified in 37 C.F.R. 1.18. If the applicant qualified for and has filed a verified statement of small entity status in accordance with 37 C.F.R. 1.27, the issue fee is one-half the amount for non-small entities. The issue fee due printed above reflects applicant's status as of the time of mailing this notice. A verified statement of small entity status may be filed prior to or with payment of the issue fee. However, in accordance with 37 C.F.R. 1.28, failure to establish status as a small entity prior to or with payment of the issue fee precludes payment of the issue fee in the amount so established for small entities and precludes a refund of any portion thereof paid prior to establishing status as a small entity.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE as indicated above. The application shall otherwise be regarded as ABANDONED. The issue fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office. Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of the notice of allowance, the issue fee is charged to the deposit account at the time of mailing of this notice in accordance with 37 C.F.R. 1.311. If the issue fee has been so charged, it is indicated above.

In order to minimize delays in the issuance of a patent based on this application, **this Notice may have been mailed prior to completion of final processing.** The nature and/or extent of the remaining revision or processing requirements may cause slight delays of the patent. In addition, **if prosecution is to be reopened, this Notice of Allowance will be vacated and the appropriate Office action will follow in due course.** If the issue fee has already been paid and prosecution is reopened, the applicant may request a refund or request that the fee be credited to a deposit account. However, applicant may request that the previously submitted issue fee be applied. If abandoned, applicant may request refund or credit to a deposit account.

In the case of each patent issuing without an assignment, the complete post office address of the inventor(s) will be printed in the patent heading and in the Official Gazette. If the inventor's address is now different from the address which appears in the application, please fill in the information in the spaces provided on PTOL-85b enclosed. If there are address changes for more than two inventors, enter the additional addresses on the reverse side of the PTOL-85b.

The appropriate spaces in the ASSIGNMENT DATA section of PTOL-85b must be completed in all cases. If it is desired to have the patent issue to an assignee, an assignment must have been previously submitted to the Patent and Trademark Office or must be submitted not later than the date of payment of the issue fee as required by 37 C.F.R. 1.334. Where there is an assignment, the assignee's name and address must be provided on the PTOL-85b to ensure its inclusion in the printed patent.

Advance orders for 10 or more printed copies of the prospective patent can be made by completing the information in Section 4 of PTOL-85b and submitting payment therewith. If use of a deposit account is being authorized for payment, PTOL-85c should also be forwarded. The order must be for at least 10 copies and must accompany the issue fee. The copies ordered will be sent only to the address specified in section 1 or 1A of PTOL-85b.

☑ Note attached communication from the Examiner.

☐ This notice is issued in view of applicant's communication filed _____

PATENT AND TRADEMARK OFFICE COPY

IMPORTANT REMINDER

Patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. See 37 CFR 1.20 (e)—(j).

FCS1688887

HARRIS

Attorney Docket SE-395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Patent Application

Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

Commissioner of Patents and Trademarks
Washington, D. C. 20231
Attention: Official Draftsman

LETTER OF TRANSMITTAL - FORMAL DRAWINGS

Sir:

Enclosed herewith for filing are the formal drawings for the subject application. The art unit number, serial number and number of drawing sheets is written on the reverse side of each drawing.

The Commissioner is hereby authorized to charge any fees to Deposit Acct. No. 08-0870. An additional copy of this sheet is enclosed.

Respectfully submitted,

William A. Troner
Registration No. 32,316
(407) 729-4511

035/D

HARRIS CORPORATION SEMICONDUCTOR SECTOR P.O. BOX 883 MELBOURNE, FLORIDA 32901

HARRIS

Attorney Docket SE-395

COMMISSIONER OF PATENTS AND TRADEMARKS

In re Patent Application

Applicant:	JAMES D. BEASOM
Serial No.:	831,384
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

CERTIFICATE OF MAILING 37 C.F.R. 1.8(a)

I hereby certify that the attached Transmittal of Formal Drawings is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

on the date indicated below.

DATE: December 20, 1988

BY: William A. Troner

William A. Troner
Reg. No 32,316
(407) 729-4511

035/D

831384

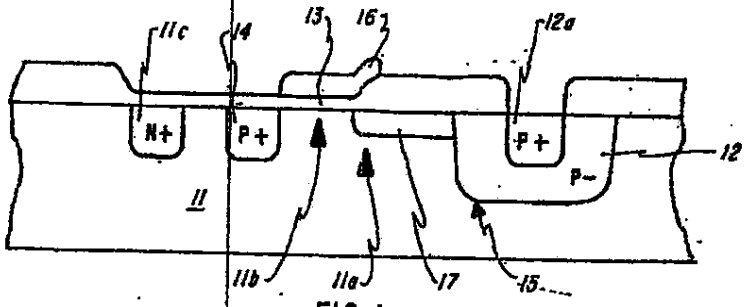


FIG. 1

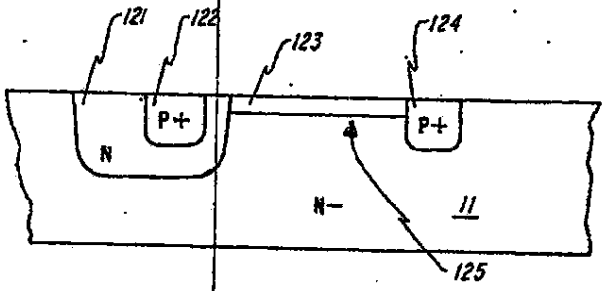


FIG. 2

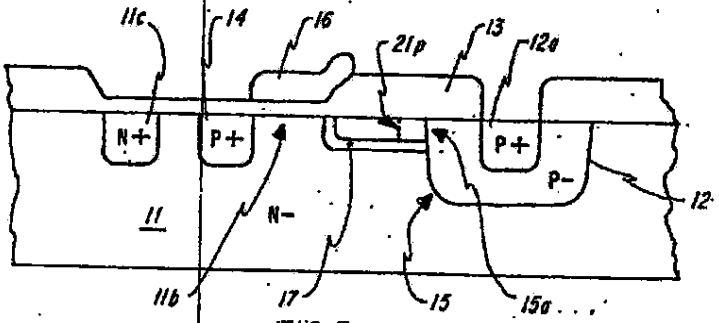


FIG. 3

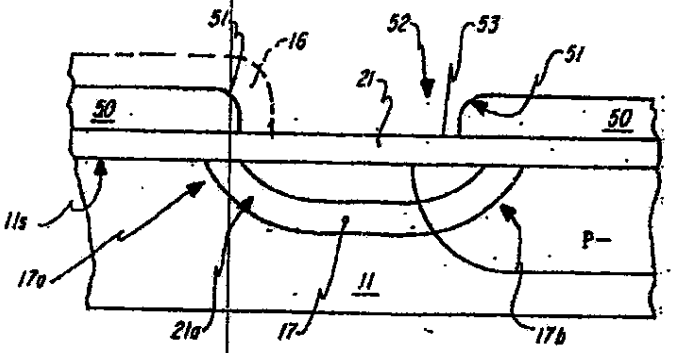


FIG. 4

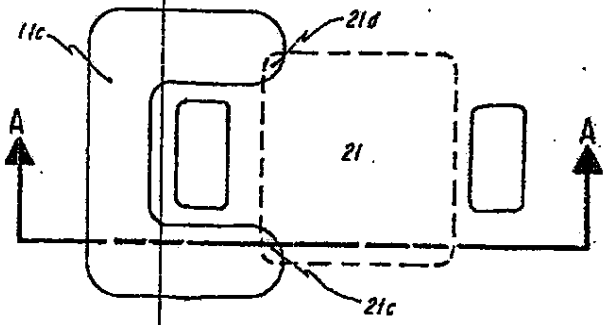


FIG. 5a

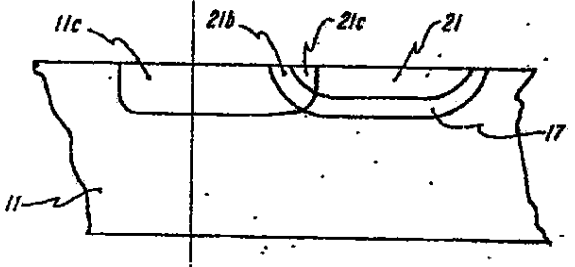


FIG. 5b

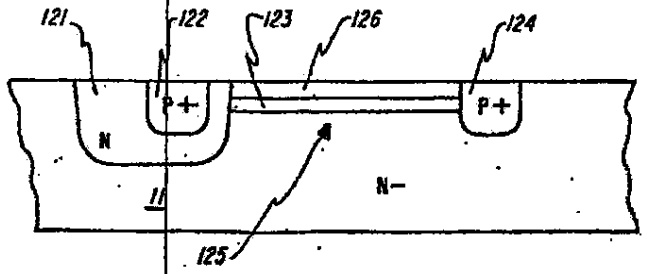


FIG. 6

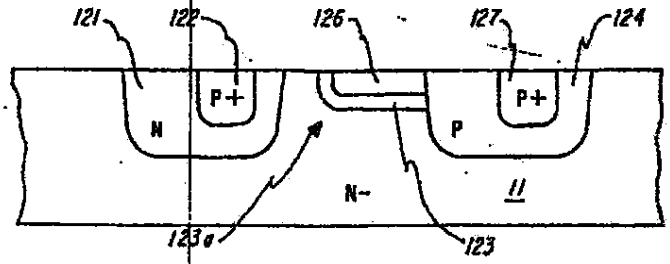


FIG. 7

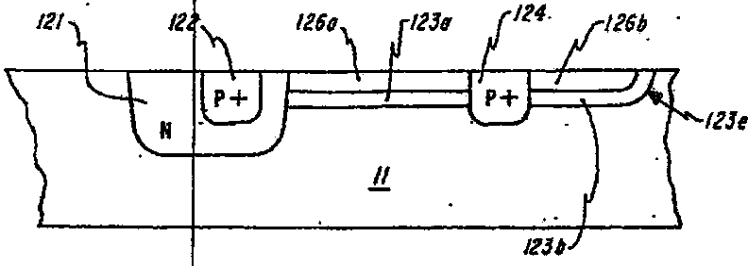


FIG. 8.

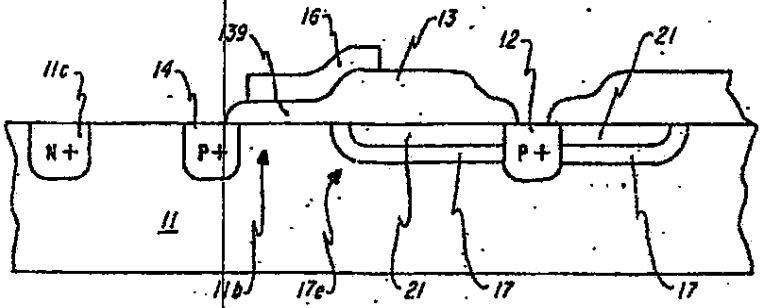


FIG. 9

ISSUE FEE TRANSMITTAL

U.S. Department of Commerce
Patent and Trademark Office

s provided in lieu of a formal transmittal and should be used for transmitting the Issue Fee. Sections 1A through 4 must be appropriate.

DRESS CHANGE — | SC/SERIAL NO.

ME

IP Code

NAME

ZIP Code

additional changes are on reverse side.

MAILING INSTRUCTIONS

All further correspondence including the Issue Fee Receipt, the Patent, and advance orders will be mailed to the addressee entered in section 1 on PTOL-85c, unless you direct otherwise by specifying the appropriate name and address in 1A below. (Note: See box 5 below for correspondence concerning maintenance fee payments.)

2A. The COMMISSIONER OF PATENTS AND TRADEMARKS is requested to apply the Issue Fee to the application identified below.

(Signature of party in interest of record) | (Date)

William A. Stoner | December 19, 1998

Note: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

SC/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
08/831,384	01/07/86	017	CLAWSON JR. J 253	10/04/88

BEASOM, JAMES D.

HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION (AS AMENDED)

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
GE-39??	357-022.000	082	UTILITY	NO	$560.00	01/04/89

1A. Further correspondence to be mailed to the following:

2B. For printing on the patent front page, list the names of not more than 3 registered patent attorneys or agents OR, alternatively, the name of a firm having as a member a registered attorney or agent. If no name is listed, no name will be printed.

1 William A. Stoner
2 Charles C. Krawczyk
3

DO NOT USE THIS SPACE

P 30328 12/30/88 831384
P 30329 12/30/88 831384

08-0870 030 142 560.00CH
08-0870 030 501 15.00CH

3. ASSIGNMENT DATA (print or type)

A. (1) ☐ This application is NOT assigned.
(2) ☒ Assignment previously submitted to the Patent and Trademark Office.
(3) ☐ Assignment submitted herewith.

B. For Printing On The Patent: (Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data below is only appropriate when an assignment has been previously submitted to the PTO or is submitted herewith. Completion of this form is NOT a substitute for filing of an assignment as required by 37 C.F.R. 1.334).

(1) NAME OF ASSIGNEE: Harris Corporation

(2) ADDRESS: (City & State or Country) Melbourne, Florida

(3) STATE OF INCORPORATION, IF ASSIGNEE IS A CORPORATION: Delaware

4. The following fees are enclosed:
☐ Issue fee ☐ Advanced order ☐ Assignment recording

The following fees should be charged to deposit acc. no. 08-0870
(PTOL-85c or additional copy of PTOL-85b must be enclosed)

☒ Issue fee ☐ Assignment recording
☒ Advanced order ☐ Any additional fees due

Number of advanced order copies requested. 10
(must be for 10 or more copies)

5. All correspondence relating to maintenance fees will be addressed to the correspondence address unless a separate "Fee Address" is provided to the Patent and Trademark Office (37 C.F.R. 1.363). A "Fee Address" may be submitted by the owner of record with the payment of the issue fee or thereafter by using form PTO-1537.

TRANSMIT THIS FORM WITH FEE

HARRIS

Attorney Docket SE-395

COMMISSIONER OF PATENTS AND TRADEMARKS

In re Patent Application

Applicant:	JAMES D. BEASON
Serial No.:	831,364
Filed:	1/07/86
For:	HIGH VOLTAGE LATERAL MOS STRUCTURE
Group Art Unit:	253
Examiner:	J. E. Clawson, Jr.

CERTIFICATE OF MAILING 37 C.F.R. 1.8(a)

I hereby certify that the attached Issue Fee Transmittal is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

BOX ISSUE FEES
COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, DC 20231

on the date indicated below.

Formal Drawings have been sent under separate cover to the Commissioner of Patents and Trademarks.

DATE: December 22, 1988

BY: William A Troner

William A. Troner
Reg. No 32,316
(407) 729-4511

033/D

PATENT NUMBER

APPLICATION SERIAL NUMBER
831,384

APPLICANT'S NAME (PLEASE PRINT)
BEASOM

IF REISSUE, ORIGINAL PATENT NUMBER

INTERNATIONAL CLASSIFICATION (INT. CL. 4)

H	0	1	L		9/80
					/
					/
					/

ORIGINAL CLASSIFICATION

CLASS	SUBCLASS
357	22

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			
357	73.8	35		

GROUP ART UNIT
253

ASSISTANT EXAMINER (PLEASE STAMP OR PRINT FULL NAME)

PRIMARY EXAMINER (PLEASE STAMP OR PRINT FULL NAME)
JOSEPH E. CLAWSON JR.

PTO 270 (10-84)

ISSUE CLASSIFICATION SLIP

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

FCS1688895

FORM PTO-875 (Rev. 3-83) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

PATENT APPLICATION FEE DETERMINATION RECORD

SERIAL NO. 831394 | FILING DATE 1-7-86

APPLICANT (FIRST NAMED) James D. Beeson

CLAIMS AS FILED - PART I

FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
TOTAL CLAIMS	25 -20=	5
INDEP. CLAIMS	4 -3=	1
☐ MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in col. 1 is less than zero, enter "0" in col. 2

	SMALL ENTITY RATE	SMALL ENTITY FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY FEE
		$170	OR		$340
	x6	$	OR	x12	$60
	x17	$	OR	x34	$34
	x55	$	OR	x110	$ 0
	TOTAL	$	OR	TOTAL	434

Amdt A

CLAIMS AS AMENDED - PART II

AMENDMENT A	(1) CLAIMS REMAINING AFTER AMENDMENT		(2) HIGHEST NO. PREVIOUSLY PAID FOR	(3) PRESENT EXTRA
TOTAL	19	MINUS **	25	-
INDEP.	4	MINUS ***	4	-
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

	SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY ADDIT. FEE
	- 5 -	$		x10 -	$
	- 15 -	$		x30 -	$
	- 50 -	$		- 100 -	$
	TOTAL ADDIT. FEE	$	OR	TOTAL	$

B

AMENDMENT B	(1) CLAIMS REMAINING AFTER AMENDMENT		(2) HIGHEST NO. PREVIOUSLY PAID FOR	(3) PRESENT EXTRA
TOTAL	19	MINUS **	25	-
INDEP.	4	MINUS ***	4	-
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

	SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY ADDIT. FEE
	- 5 -	$		x10 -	$
	- 15 -	$		x30 -	$
	- 50 -	$		- 100 -	$
	TOTAL ADDIT. FEE	$	OR	TOTAL	$

AMENDMENT C	(1) CLAIMS REMAINING AFTER AMENDMENT		(2) HIGHEST NO. PREVIOUSLY PAID FOR	(3) PRESENT EXTRA
TOTAL	19	MINUS **	25	-
INDEP.	4	MINUS ***	4	-
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

	SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE		OTHER THAN A SMALL ENTITY RATE	OTHER THAN A SMALL ENTITY ADDIT. FEE
	x5 -	$		x10 -	$
	x15 -	$		x30 -	$
	x50 -	$		x100 -	$
	TOTAL ADDIT. FEE	$	OR	TOTAL	$

* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.

** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest No. Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest No. Previously Paid For" (Total or Indep.) is the highest number found in the appropriate box in Col. 1.

PTO-1130 (Rev. 3-83) 831384

PALM III APPLICATION FILE DATA CODING SHEET

U.S. DEPARTMENT OF COMMERCE—PATENT & TM OFFICE | PREPARED BY: SH | DATE: 5-20-86

FORMAT NO. 2 Serial No.	TYPE APPL	FILING DATE (Month / Day / Year)	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWINGS	ASGT?	TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE RECEIVED	SECURITY CASE?	FOREIGN LICENSE?
06	1	02 / 07 / 86		154	428	005	1	025	003	0	0434	N	Y

FORMAT NO. 3 — ATTORNEY DOCKET NUMBER (12 spaces): SE-395 — Atty.'s Reg. Nos. — ☐ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 4 Applicant's Name & Address — ☐ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 5 Title of Invention — ☑ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 6&7 Correspondence Address — ☑ APPL. PAPERS ☐ CODING SHEET

FORMAT NO. 8

	CONTINUITY CODE	PARENT APPLICATION SERIAL NUMBER	PARENT FILING DATE (Month / Day / Year)	STATUS CODE	PARENT PATENT NUMBER
RECORD 801		0			
RECORD 802		0			
RECORD 803		0			
RECORD 804		0			
RECORD 805		0			
RECORD 806		0			
RECORD 807		0			
RECORD 808		0			
RECORD 809		0			
☐ MORE ON SUPPLEMENTAL CODING SHEET — RECORD 810		0			

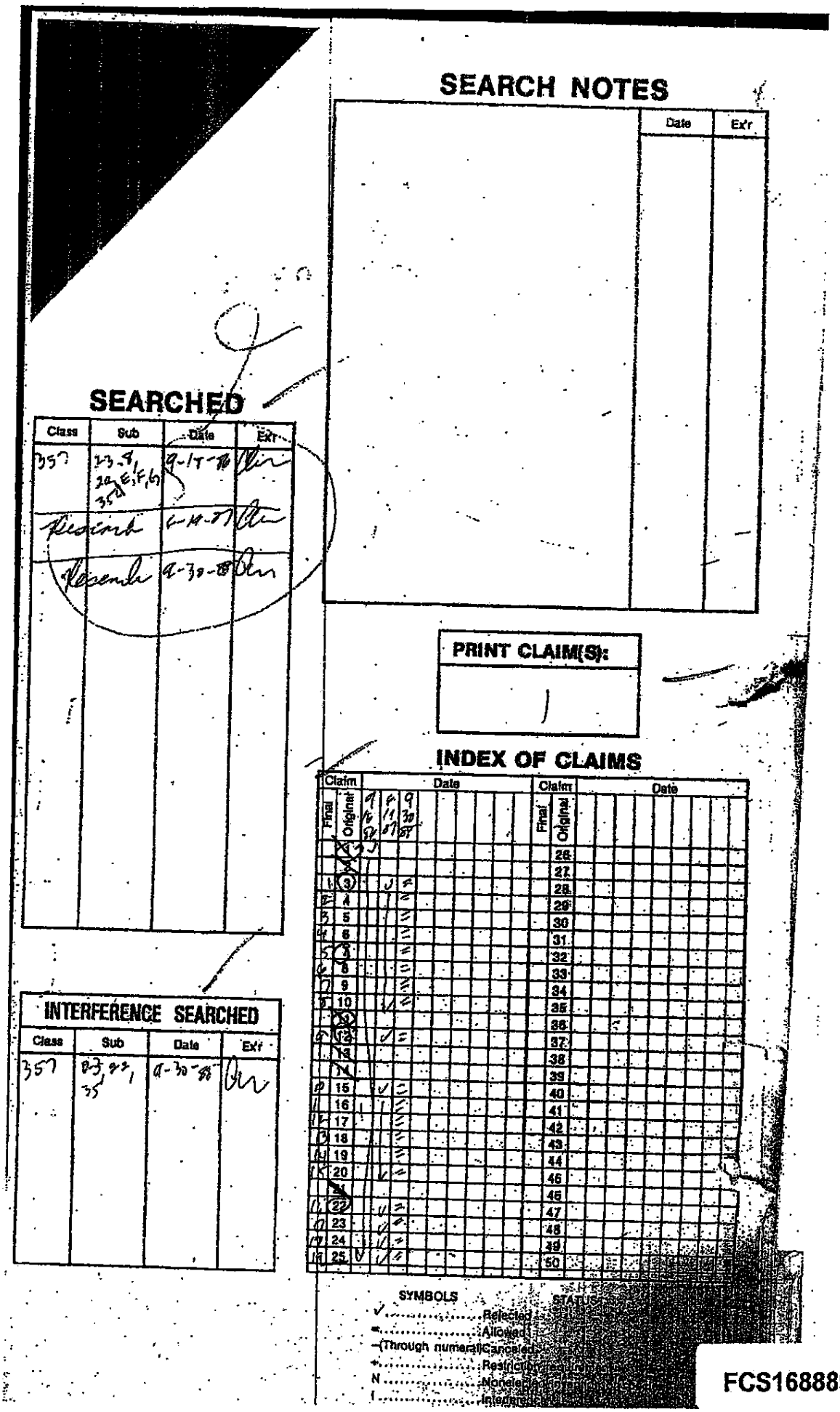
FORMAT NO. 9

FOREIGN PRIORITY CLAIMED? ☐ YES ☒ NO

☐ APPLICATION PAPERS

	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FILING DATE (Month / Day / Year)
RECORD 901			
RECORD 902			
RECORD 903			
RECORD 904			
RECORD 905			
RECORD 906			
RECORD 907			
RECORD 908			
RECORD 909			
☐ MORE ON SUPPLEMENTAL CODING SHEET — RECORD 910			

FCS1688897



SEARCH NOTES

	Date	Ex'r

SEARCHED

Class	Sub	Date	Ex'r
357	23-9, 29 E,F,G 35	9-17-98	
Reissued		6-14-99	
Reissued		9-30-08	

PRINT CLAIM(S):

INDEX OF CLAIMS

Claim Final	Claim Original	Date	Claim Final	Claim Original	Date
		9/30/08		26	
	2			27	
	3			28	
	4			29	
	5			30	
	6			31	
	7			32	
	8			33	
	9			34	
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	14			39	
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	21			46	
	22			47	
	23			48	
	24			49	
	25			50	

SYMBOLS

STATUS

✓ ..... Rejected
= ..... Allowed
– (Through numeral) ..... Canceled
. ..... Restricted
N ..... Nonelected
I ..... Interference

INTERFERENCE SEARCHED

Class	Sub	Date	Ex'r
357	23, 29, 35	9-30-98	

FCS1688898

831384

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[redacted]

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APR 14 1996
GROUP 150

Entered

CONTENTS

	1.	Applications ✓ papers.	
	2.	~~Ltr (3 Mo)~~	Sept 25, 1986 ~~(11.9)~~ 12
4/7	3.	~~Reg Ext~~ March 23, 1987 ~~(3 mos~~	
4/7	4.	~~Amdt A~~ March 23, 1987	
	5.	~~2nd Ltr (3 Mo)~~ July 10, 1987 OT	4/22
12/7	6.	~~Reg Ext~~ Dec 8, 1987 ~~(2 mos~~	
"	7.	~~Amdt B~~ Dec 8, 1987	
2/89	8.	~~FR (3 Mo)~~ March 9, 1988 (DW)	
	9.	~~PTOL-413 (8-2-88)~~	
9-14	10.	~~Reg Ext~~ ✓ Sept 9 1988 ~~(3 mos~~	
"	11.	~~Amdt C~~ (E) Sept 9, 1988	
"	12.	Notice of Appeal Sept 9, 1988	
	13.	~~PTOL-37 (7)~~ Oct 4, 1988 OT	10/3
	14.	Formal Drwgs (3 sets) 12/27/88	
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